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**GEORGIA TECH GT-VTHR
VLSI DESIGN VERIFICATION DOCUMENT**

VLSI DEVELOPMENT REPORT
REPORT NO. VDR-0142-90-007
FEBRUARY 15, 1991

**GUIDANCE, NAVIGATION AND CONTROL
DIGITAL EMULATION TECHNOLOGY LABORATORY**

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COMPUTER ENGINEERING RESEARCH LABORATORY

Georgia Institute of Technology
Atlanta, Georgia 30332-0540

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FEBRUARY 15, 1991

Rafik Braham

COMPUTER ENGINEERING RESEARCH LABORATORY

Georgia Institute of Technology
Atlanta, Georgia 30332-0540

Eugene L. Sanders
USASDC
Contract Monitor

Cecil O. Alford
Georgia Tech
Project Director

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Georgia Tech Research Corporation (GTRC)
Centennial Research Building
Atlanta, Georgia 30332

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GEORGIA TECH GT-VTHR VLSI DESIGN VERIFICATION DOCUMENT

INTRODUCTION

There are eleven (11) Georgia Tech VLSI designs (see Table 1) in the AHAT Program. Each of these designs has been produced by Georgia Tech using the Genesil Silicon Compiler. Each design has passed the design verification process at Silicon Compiler Systems / Mentor Graphics and each has been fabricated in a bulk CMOS process (fabrication of certain chips was not complete when this document was released). Each of the Georgia Tech designs listed in Table 1 is being delivered to USASDC and to the Harris Corporation for conversion and fabrication in a rad-hard process. The program under which this work is done is AHAT (Advanced Hardened Avionics Technology). This document includes design information for the Georgia Tech thresholding chip, GT-VTHR.

Table 1. Georgia Tech Chip Set for AHAT

Design	DV Passed	Tape Delivered	Fabricated	Tested
GT-VFPU/1A	1/17/89	8/3/90	5/19/89	4/4/90
GT-VNUC				
GT-VTF				
GT-VTHR	12/11/90	2/15/91		
GT-VCLS	1/26/90	7/12/90	7/13/90	
GT-VCTR	2/8/90	7/12/90	7/13/90	
GT-VIAG				
GT-VDAG				
GT-VSNI	1/17/89	5/23/90	4/14/89	4/4/90
GT-VSM8	1/17/89	6/8/90	5/6/89	4/4/90
GT-VSF	9/12/89	7/19/90	7/13/90	

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DV CHECKLIST

1. DV CONTROL NUMBER : _____

2. CUSTOMER INFORMATION

Customer Name : Georgia Tech / CERL Chip Name : GT-VTHR

Address : 400 Tenth Street FAX : (404) 894-3120

CRB Room 377

Atlanta, GA 30332-0540

Project Manager : Dr. C. O. Alford Phone : (404) 894-2505

Design Engineer : Rafik Braham Phone : (404) 894-2527

_____ Phone : _____

Test Engineer : Joseph I. Chamdani Phone : (404) 894-2527

3. SERVICES INFORMATION

xx Design Verification Service only. PO # _____

_____ Prototype Service and Design Verification. PO # _____

_____ 1.8% Maintenance

_____ SCS Test _____ Foundry Test _____ Customer Test

When DV is complete, send verified physical database tape to

Customer Y N Silicon Vendor Y N

4. DV CONTACT : Ying Chow Phone : (408) 371-2900

5. REGRESSION

5. 1. GENESIL Version : 8.0.2
5. 2. Name of Session Log from recompile : rebuild.LOG
5. 3. Include DV regression.CMD : DV_regression.001 (simulation and timing)
5. 4. Size of database (MB) : 124 Guess Density : 6250 1600 TK50
Tar xx wbak Apollo Cartridge
(compressed) Sun Cartridge xx

6. FUNCTIONAL INFORMATION (check when included)

6. 1. Number of Transistors : xx
6. 2. Key Parameters : xx Testing ____
6. 3. DV pin description : xx Testing ____
6. 4. Block Diagram : xx Testing ____
6. 5. Functional Description : xx Testing ____
6. 6. Timing Diagrams at Pins : xx Testing ____
6. 7. Annotated Views : xx Testing ____
6. 8. Chip Text Specification on tape : xx
(vthr_spec.012)
- Annotated Schematics : xx Testing ____
Density: 6250____ 1600____ TK50____
Apollo Cartridge____
Sun Cartridge xx

7. PHYSICAL INFORMATION

7. 1. Fabline Name : HPI CN10A
Customer-Specific : Y N Fabline GENECAL Directory on tape : Y N
Fabline GENESIL Directory on tape : Y N
Fabline Calibration Status : Production : xx Beta : Alpha :
NOTE: If not a production fabline, then approval from SCS is required.
7. 2. Plots: (check when included or indicate filename)
Chip Route (D size) : xx Bonding Diagram (B size) : xx
Route Filename : rt PLOT 1.031 Bonding Filename : bd PLOT 1.031
7. 3. Die Size : Reported Die Size : 404.9 x 400.0 square-mils
Maximum Acceptable Die Size (+/- 2%) : 435 x 435 square-mils
Minimum Acceptable Die Size (+/- 2%) : 300 x 300 square-mils
7. 4. GENESIL Package Name : CPGA100hp Spec included? Y N
Cavity/Well Size : 470 mils by 470 mils
Non-GENESIL Supplied Package? Y N Text Spec included on tape? Y N
Vendor Name/Part # : KYOCERA KD-P85989 Foundry Approval? Y N
7. 5. External Block: none
7. 6. LRAM: Y N LROM: Y N LPLA: Y N LogicCompiler Blocks: Y N
7. 7. Test Pad (PM Pad) is included? Y N (Required for PS)

7. 8. Power Pad : VCC: Core 2 VSS: Core 2
 Ring 9 Ring 6

NP protection for nwell pad? Y N

TTL output pads or N Protection for inputs? Y N
 If yes, have you received silicon vendor approval? Y N

Error in PADRING.033 (PADRING.DRC)? Y N Hardcopy attached? Y N

ESD requirements _____ Approved by SCS? Y N

8. ELECTRICAL INFORMATION

8. 1. Chip Frequency Specified in netlist : 2.67 MHz Target frequency : 2.67 MHz

8. 2. Power Dissipation: GENESIL = 0.85 W at 10 MHz Spec = _____ W at _____ MHz

8. 3. Operating Voltage: from 4.5 Volts to 5.5 Volts

9. SIMULATION

9. 1. Number of Clocking Regimes : 1

	Clock Pad Name	DIV/NO DIV	Ext Clock Name	Int PHASE A/PHASE B Name
1.	<u>pixel_clk</u>	<u>NO DIV</u>	<u>Pixel_clk</u>	<u>PHASE A / PHASE B</u>
2.	_____	_____	_____	_____
3.	_____	_____	_____	_____
4.	_____	_____	_____	_____
5.	_____	_____	_____	_____

9. 2. Simulation Setup Files:

Name : none / default Listings attached : _____

Description : _____

Affected Tests : _____

Name : _____ Listings attached : _____

Description : _____

Affected Tests : _____

Name : _____ Listings attached : _____

Description : _____

Affected Tests : _____

Name : _____ Listings attached : _____

Description : _____

Affected Tests : _____

9. 3. Test Vector Set:

Total No. of Vectors : 32,707

NOTE : Test vectors written one phase per vector have a maximum test frequency on the IMS Tester of 10 MHz. Test vectors written one cycle per vector have a maximum test frequency on the IMS Tester of 20 MHz.

1. Name : adap simp man.col.083 No of vectors : 4,425
Description : tests adaptive and simple thresholding

Portions of Chip Tested : all

Pass with GFL model? yes
Pass with GSL model? yes Use for PS testing? Y N
Pass Fight Test? _____

2. Name : adapt4 5 man.col.083 No of vectors : 1,441
Description : tests adaptive thresholding

Portions of Chip Tested : all

Pass with GFL model? yes
Pass with GSL model? yes Use for PS testing? Y N
Pass Fight Test? _____

3. Name : adapt 4 man.col.083 No of vectors : 731
Description : tests adaptive thresholding

Portions of Chip Tested : all

Pass with GFL model? yes
Pass with GSL model? yes Use for PS testing? Y N
Pass Fight Test? _____

4. Name : adapt 2f man.col.083 No of vectors : 2,576
Description : tests adaptive thresholding (two frames)

Portions of Chip Tested : all

Pass with GFL model? yes
Pass with GSL model? yes Use for PS testing? Y N
Pass Fight Test?

5. Name : adapt_adj_man.col.083 No of vectors : 3,360
Description : tests adaptive and adjusted thresholding

Portions of Chip Tested : all

Pass with GFL model? yes
Pass with GSL model? yes Use for PS testing? Y N
Pass Fight Test?

6. Name : adj2_man.col.083 No of vectors : 2,007
Description : tests adjusted thresholding mode

Portions of Chip Tested : all

Pass with GFL model? yes
Pass with GSL model? yes Use for PS testing? Y N
Pass Fight Test?

7. Name : fifos_man.col.083 No of vectors : 1,557
Description : tests the fifo pipe structure

Portions of Chip Tested : all

Pass with GFL model? yes
Pass with GSL model? yes Use for PS testing? Y N
Pass Fight Test?

8. Name : host_inter_man.col.083 No of vectors : 56
Description : tests the host interface

Portions of Chip Tested : host interface

Pass with GFL model? yes
Pass with GSL model? yes Use for PS testing? Y N
Pass Fight Test?

9. Name : simp adap man.col.083 No of vectors : 2,084
 Description : tests simple and adaptive thresholding modes

Portions of Chip Tested : all

Pass with GFL model? yes
 Pass with GSL model? yes Use for PS testing? Y N
 Pass Fight Test?

10. Name : simp adj adap.col.083 No of vectors : 13,044
 Description : tests all three thresholding modes

Portions of Chip Tested : all

Pass with GFL model? yes
 Pass with GSL model? yes Use for PS testing? Y N
 Pass Fight Test?

11. Name : simp man.col.083 No of vectors : 1,426
 Description : tests simple thresholding

Portions of Chip Tested : all

Pass with GFL model? yes
 Pass with GSL model? yes Use for PS testing? Y N
 Pass Fight Test?

9. 4. IMS Grouping within limitation? Y N (Required for PS only)

9. 5. Tester clock frequency = 2.67 MHz

9. 6. Signals that must be glitch free: Y N

Signal Name	Ran GSL with glitch detection feature on?
1. <u>Begin frame out</u>	<u>Y</u> N
2. <u>Begin row out</u>	<u>Y</u> N
3. <u>End frame out</u>	<u>Y</u> N
4. <u>End row out</u>	<u>Y</u> N
5. <u>N dr</u>	<u>Y</u> N
6. <u> </u>	<u>Y</u> N
7. <u> </u>	<u>Y</u> N
8. <u> </u>	<u>Y</u> N
9. <u> </u>	<u>Y</u> N

10. TIMING ANALYSIS

10. 1. System Environment

Temperature Coefficient: 35 Degrees C / Watt (theta JA)Operating Temp : from 0⁰ C (min) to 70⁰ C (max)Operating Voltage : from 4.5 V (min) to 5.5 V (max)room junction temp = $25 + (\text{theta JA} * \text{Power}) = \underline{55}$ degrees Cmaximum junction temp = maximum ambient temp + (theta JA * Power) = 100 degrees C

10. 2. Reports (Include the following reports)

(required for PS)*

guaranteed corner

5.0V

room junc temp

(required for PS)*

guaranteed corner

min operating V

max junction temp

typical corner

min operating V

max junction temp

Cycle : xxSetup/Hold : xxOutput Delay : xxViolation : xxCycle : xxSetup/Hold : xxOutput Delay : xxViolation : xxCycle : xxSetup/Hold : xxOutput Delay : xxViolation : xx

10. 3. Timing Setup Files:

Name : worstcase.040 Listings attached : yesTemperature : 100 degrees C Voltage : 4.50 VDescription : worst case condition, maximum junction temperature, minimum operating voltageName : nominal.040 Listings attached : yesTemperature : 55 degrees C Voltage : 5.00 VDescription : nominal condition, room junction temperature, 5.0 V operating voltage

Name : _____ Listings attached : _____

Temperature : _____ Voltage : _____

Description : _____

Name : _____ Listings attached : _____

Temperature : _____ Voltage : _____

Description : _____

10. 4. Critical Boundary Conditions:

List critical paths here or annotate the timing report.

Attach additional pages if needed.

Clock Name :	<u>Pixel clk</u>			
	report	limit (+/-5%)	report	limit (+/-5%)
1. Phase 1 High	<u>198.6 ns</u>	<u>210 ns</u>	<u> </u>	<u> </u>
2. Phase 2 High	<u>185.9 ns</u>	<u>210 ns</u>	<u> </u>	<u> </u>
3. Symmetric Cycle	<u>397.1 ns</u>	<u>420 ns</u>	<u> </u>	<u> </u>
4. Minimum Cycle	<u>384.5 ns</u>	<u>420 ns</u>	<u> </u>	<u> </u>

Outputs

	Signal Name	load (pF)	delay	limit
1.	<u>Begin frame out</u>	<u>50.00</u>	<u>25.9 ns</u>	<u>30 ns</u>
2.	<u>Begin row out</u>	<u>50.00</u>	<u>25.8 ns</u>	<u>30 ns</u>
3.	<u>End frame out</u>	<u>50.00</u>	<u>25.7 ns</u>	<u>30 ns</u>
4.	<u>End row out</u>	<u>50.00</u>	<u>25.7 ns</u>	<u>30 ns</u>
5.	<u>Pixel out[15:0]</u>	<u>50.00</u>	<u>26.1 ns</u>	<u>30 ns</u>
6.	<u> </u>	<u> </u>	<u> </u>	<u> </u>
7.	<u> </u>	<u> </u>	<u> </u>	<u> </u>
8.	<u> </u>	<u> </u>	<u> </u>	<u> </u>
9.	<u> </u>	<u> </u>	<u> </u>	<u> </u>

Inputs

	Signal Name	setup report / limit	hold report / limit
1.	<u> </u>	<u>/</u>	<u>/</u>
2.	<u> </u>	<u>/</u>	<u>/</u>
3.	<u> </u>	<u>/</u>	<u>/</u>
4.	<u> </u>	<u>/</u>	<u>/</u>
5.	<u> </u>	<u>/</u>	<u>/</u>
6.	<u> </u>	<u>/</u>	<u>/</u>
7.	<u> </u>	<u>/</u>	<u>/</u>
8.	<u> </u>	<u>/</u>	<u>/</u>
9.	<u> </u>	<u>/</u>	<u>/</u>

10. 5. Hold Time Violations : none (At 2.0 nsec.)

11. DC CHARACTERISTICS

PARAMETERS	DESCRIPTION	CONDITIONS 0 to 70	CONDITIONS -55 to +125	MIN	MAX
DATA PAD INPUT ONLY					
VIH	Input High Voltage			2.0V	
VIL	Input Low Voltage				0.8V
IIL	Input Leakage	VSS < Vin < VDD	VSS < Vin < VDD	-10uA	10uA
CIN	Input Capacitance				6.0pf
DATA PAD OUTPUT ONLY					
VOH	Output High Voltage	VDD= 4.5V IOH=-2.2	VDD= 4.5V IOH=-2mA	2.4V	
VOL	Output Low Voltage	VDD= 4.5V IOL= 6mA	VDD= 4.5V IOL= 5mA		0.4V
IOZ	Output Leakage current(high Z)	VSS < Vout < VDD	VSS < Vout < VDD	-10uA	10uA
COUT	Output Capacitance				7.0pf
DATA PAD INPUT/OUTPUT					
VOH	Output High Voltage	VDD= 4.5V IOH=-2.2	VDD= 4.5V IOH=-2mA	2.4V	
VOL	Output Low Voltage	VDD= 4.5V IOL= 6mA	VDD= 4.5V IOL= 5mA		0.4V
VIH	Input High Voltage			2.0V	
VIL	Input Low Voltage				0.8V
IOZ	Output leakage current (high Z)	VSS < Vout < VDD	VSS < Vout < VDD	-10uA	10uA
CIO	Input/Output Capacitance				7.0pf
CLOCK PAD					
VIH	Input High Voltage			3.9V	
VIL	Input Low Voltage				0.6V
IIL	Input Leakage	VSS < Vin < VDD	VSS < Vin < VDD	-10uA	10uA
CIN	Input Capacitance				15pf

NOTE: All parameters at a supply voltage of VDD = 5V (+/- 10%).

12. CUSTOMER COMMENTS

Pre-Verification Comments (10/24/90)

The GSL simulation failed on 10 test vectors files (see section 9.3). The source of the GSL errors was determined originating from clocks etc/sp interface block which is a Logic Compiler block. If the compiler option of this block is changed to Standard Compiler all the test vector files pass GSL simulation. Therefore it is assumed that errors must have occurred inside the GENESIL Autologic program, i.e., improper optimization or realization of the actual circuitry. This problem must be fixed by SCS / Mentor Graphics and approved by Georgia Tech / CERL prior to sending the chip database to silicon foundry.

Post-Verification Comments (12/11/90)

The above problem has been fixed by Mentor Graphics. All test vector files now pass GSL simulation.

13. CUSTOMER APPROVAL

The undersigned understands that if any design changes are initiated by the Customer subsequent to this sign-off, the Customer is liable for any charges imposed by Silicon Compiler Systems as agreed to in either the Design Verification Terms & Conditions or the Prototype Services Terms & Conditions. In addition, such changes require the DV process to be started from the beginning, which results in extended DV schedules.

Customer Approval : Joseph I. Chamdani *J.I. Chamdani* Date 10 / 24 / 90

Title : Research Engineer I

14. SCS APPROVAL

Pre-Verification Comments

SCS Approval : _____ Date ____/____/____
Regional Field Application Consultant

SCS Approval : _____ Date ____/____/____
Technical Support Team Leader

GT-VTHR : Thresholding Chip

1. Introduction

Thresholding is the last stage in preprocessing the pixel intensities before they are actually employed for useful processing. Normally, this function comes just before clustering..

2. Functional Description

The thresholding chip provides three types of thresholding: simple, adjusted and adaptive. It is composed of seven modules: adjust, adapt, host_stuff, store, store_ctrl, clocks_etc, and output (see Figure 1). Note that all figures referred to can be found in Appendix A.

2. 1. Module adjust

This module contains the circuitry necessary to compute the threshold for both simple and adjusted modes which are explained below.

2. 1. 1. Simple Thresholding

In this mode, all the pixels are compared to a fixed threshold. The threshold value is preloaded by the host into a 16-bit register reserved for this purpose. This value may change on a frame basis.

2. 1. 2. Adjusted Thresholding

The threshold value used in simple thresholding maybe too high or too low and thus not appropriate. One way to test the "appropriateness" of this value is to count, on a frame basis, the number of pixels whose intensity values exceed the threshold (Figure 2). If this number (N_0) is too high then the threshold is increased. If it is too low however, the threshold is decreased. Therefore two values are needed to control the number of supra-threshold pixels: a lower bound (N_1) and an upper bound (N_2). At the end of each frame, the number of supra-threshold pixels is compared against the upper and lower bounds N_1 and N_2 , and the threshold is adjusted accordingly. If $N_1 < N_0 < N_2$, then the threshold is left unchanged (Figure 3).

N_1 and N_2 are loaded by the host, and they can be changed on a frame basis. The value of N_0 is made accessible to the outside of the chip. The host may use it to determine appropriate values for N_1 and N_2 . Also the host may use the value of N_0 to compute a new threshold. This threshold can be loaded by the host processor and used in the simple thresholding mode.

A block diagram of the adjusted threshold hardware (combined with simple threshold) is shown in Figure 3 and Figure 4.

2. 2. Module adapt

Most of the chip circuitry consists of hardware necessary for the implementation of the adaptive thresholding algorithm. According to this algorithm, for every pixel, a threshold value is computed based on the intensities of the 8 surrounding pixels. Generally speaking, the threshold value is taken

as the average of pixel intensity plus some noise margin. Mathematically, this threshold value (theta) can be written as:

$$\theta = k_1 \times E(\text{pixel_set}) + k_2 \times L_1(\text{pixel_set}) + k_3, \quad (1)$$

where E denotes the average, L_1 the usual L_1 norm, namely $\sum_{i=0}^7 |X_i - E(\text{pixel_set})|$ and pixel_set the set of the 8 pixels neighboring to the current pixel. Let us work out an example to illustrate these ideas.

Consider Figure 5, the pixels are designated by their arrival time (in clock cycles) relative to the present. At $t = 0$, the pixel $XZ^0 = X$ is being received and all the information required to compute the threshold for XZ^{-130} is available. The pixel_set of equation (1) consists of:

$$\text{pixel_set} = \{XZ^{-258}, XZ^{-257}, XZ^{-256}, XZ^{-131}, XZ^{-129}, XZ^{-3}, XZ^{-2}, XZ^{-1}\}.$$

Assuming uniform distribution, the average can be written as:

$$E = (XZ^{-258} + XZ^{-257} + XZ^{-256} + XZ^{-131} + XZ^{-129} + XZ^{-3} + XZ^{-2} + XZ^{-1}) \div 8. \quad (2)$$

The partial sums involved in the computation of thresholds are indicated in Figure 6(a). Because thresholds of some neighboring pixels share partial sums, the hardware is optimized to exploit this feature. Figure 6(b) shows how this is possible. At least 4 pipeline stages are necessary to compute the 8-point sums of E , and meet the processing requirements.

Figure 7 represents the reservation table for the 4-stage pipeline. As can be seen from the figure, once the first 8-point sum is delivered, a new sum is delivered every cycle thereafter, and the pipeline becomes 100% full.

The computation of L_1 can proceed only when the average becomes available. L_1 can explicitly be written as:

$$L_1 = |X_0 - E| + |X_1 - E| + |X_2 - E| + |X_3 - E| + |X_4 - E| + |X_5 - E| + |X_6 - E| + |X_7 - E|. \quad (3)$$

Figure 8 summarizes how L_1 is computed. Figure 9 and Figure 10 show further detail of the hardware implementation.

Figure 11 shows a block diagram and Figure 12 shows the details of the hardware circuitry that computes the adaptive threshold.

2.3. Module host_stuff

This module consists of the circuitry necessary to reset the chip, load constants into it, and read out data either for diagnostic purposes or for deciding on the thresholding mode to be used. Three blocks: `reg0`, `reg1`, and `reg2` contain latches to store data loaded by the host (Figure 13 (a), (b), (c) respectively). The "controls" block, shown in Figure 14(a), selects the thresholding mode according to Table 1 and 2. The "decoder" block (Figure 14(b)), decodes the address to select which constant the host is attempting to write.

Under "host_stuff" module, there is another module called "interface". This module supports an asynchronous interface protocol. This module was imported from the spatial filtering chip (GT-VSF). The main role of the module is to generate the handshake signals `read`, `write`, `data_dis`, and `dr_dis` (Figure 15). The details of this module are described in the GT-VSF document, and the implementation details are shown in Figure 16. A simplified timing diagram of the protocol is given in Figure 17.

2. 4. Module store

This module contains 2 FIFOs 16-bit wide and 128-word deep each, and associated control. Figure 18 illustrates its organization in a block diagram form. Figure 19 shows the implementation details of the FIFOs structure.

2. 5. Module store_ctrl

This module consists of the circuitry that controls the FIFOs. This module was imported from the spatial filtering chip. Its implementation details can be found in the GT-VSF design document. The FIFOs structure (in "store" module) is referred to as "pipe" in the spatial filtering literature.

2. 6. Module clocks_etc

This module uses the intensity stream synchronization signals (end/begin row, end/begin frame) to detect the edges (first/last row/column). Based on the edge conditions, appropriate signals are generated to output the correct result (the output intensity is zero for the edges). Figure 20 and 21 show the various blocks of which "clock_etc" module is composed.

2. 7. Module output

This module contains the necessary circuitry to output pixel intensity properly, based on the thresholding algorithm mode, threshold value(s), and validity of the pixel. A "dead" pixel is an invalid pixel which occurs between the last pixel of a row and the first pixel of the next row/frame. At every dead pixel this module forces the output pixel intensity to zero ($\text{Pixel_out}[15:0] = 0$). This module contains the following blocks:

- mux0** : selects the threshold value to be used (Figure 22(a)).
- mux1** : selects the intensity output ($\text{Pixel_out}[15:0]$). The logical circuits are shown in Figure 23.
- neuron** : compares the pixel intensity to the threshold value (Figure 22(b)).
- inverters** : a bank of 16 inverters to invert the threshold value and send it to "neuron" block Figure 24(a)).
- delay** : delays the pixel intensity by 4 cycles (Figure 24(b)).
- state_mach** : this block is a state machine that detects non valid pixels; when the output pixel intensity is not valid, $\text{Pixel_out}[15:0] = 0$ appears on the intensity bus; Figure 25 shows the logical diagram of the "state_mach" block.

3. Computational Model

The thresholding chip is slightly complicated in terms of the numerical computations involved within the chip. Omitting some implementation details, the computational model can be described as follows.

Eight 16-bit integer (positive) numbers are added together to yield a 19-bit sum. This number, which will be called $E(x)$ (for average) consists in reality of 2 fields. The 3 rightmost bits (LSBs) can be considered a fraction (the result of a division by 8). The remaining 16-bit field is the integer part of $E(x)$.

The same eight 16-bit numbers are subtracted from $E(x)$ each, and the absolute values of the 8 resulting differences are then added together. The result is a 21-bit number (18-bit integral, 3-bit fraction). This result is the L1 norm given by (3).

Next $E(x)$ is multiplied by k_1 , which is a 16-bit real number such that $0 \leq k_1 < 2$. The result is 35-bit long. The 14 LSBs are dropped, the final result is a 21-bit long (17-bit integral part, 4-bit fraction) positive number. It will be called $Prod_1$.

The norm L_1 is multiplied by k_2 , which is a 16-bit real number such that $-2 < k_2 < 2$. The result is 37-bit long. The 13 LSBs are dropped and the final result is a 24-bit number that will be called $Prod_2$. Next $Prod_1$ is added to $Prod_2$ and the result, 25-bit number, is added to k_3 (a 16-bit signed magnitude number).

The result is 26 bits long (including a sign bit). The 4 LSBs are truncated. Then bits 20 to 16 are ORed to yield $\theta[16]$. The sign and bits 15 to 0 are passed without change. The final result is thus $\theta[16:0]$.

It is this number that is compared to the incoming pixel intensity, in case of course adaptive threshold mode is being employed.

Figure 26 is a diagram summary of the algorithm just described. Note that if simple or adjusted threshold mode is used, then the computation is straightforward. In particular there is no truncation involved.

4. Signal Descriptions

Pixel_clk: main clock. This clock is internally divided into standard non-overlapping two phase clocks (Phase_A and Phase_B).

Begin_row_in, End_row_in, Begin_frame_in, End_frame_in are active high synchronization inputs with VB(t) timing characteristics. **Begin_row_out, End_row_out, Begin_frame_out, End_frame_out** are active high synchronization outputs with SA(t) timing characteristics. These signals are described in detail in the "Signal Processing Host Interface Specifications" document. Their timing characteristics is VB(t).

Pixel_in[15:0] is a 16-bit input bus for pixel intensity (VB(t)). **Pixel_out[15:0]** is a 16-bit output bus for pixel intensity (SA(t)).

Data[15:0], Address[3:0], Ds[3:0], Id[3:0], Ios, Ode, N_dr are host interface signals. The bidirectional Data[15:0] bus (input VA(t) and output WA(t)) provides separate (from pixel intensity) write/read of: k_1, k_2, k_3 , fixed threshold values (for simple and adjusted threshold modes, and upper threshold value), counter max and min (N_1 and N_2 for adjusted), and for reading counter output N_0 and the running sum value. Other host interface signals are: four address lines Address[3:0], four device select lines Ds[3:0], four chip identification bits Id[3:0], input/output select Ios, read/write select Ode, and an acknowledge signal N_dr.

Other signals are: **N_reset** (active low chip reset line), **Test** (test mode enable input), and **Theta16** (connected to $\theta[16]$ and used for testing purposes).

A complete list of pins with their timing attributes can be found in Appendix B.

5. Manufacturing Test

To improve the observability of the chip, the computed threshold is made accessible externally. The threshold least significant 16 bits appear on the host data bus when "test=1" and when the host enables the chip for read (Figure 27).

Twelve GENESIL test vector files have been created to provide manufacturing test vectors (a total of 32,707 vectors). These files can be found in the chip database:

adapt4_man.089	: tests adaptive thresholding.
adapt4_5_man.089	: tests adaptive thresholding.
adapt_simp_man.089	: tests adaptive and simple thresholding.
adapt_2f_man.089	: tests adaptive thresholding (2 frames).
adapt_adj_man.089	: tests adaptive and adjusted thresholding.
adj2_man.089	: test adjusted thresholding mode.
adj_man.089	: test adjusted thresholding.
simp_man.089	: test simple thresholding.
simp_adap_man.089	: test simple and adaptive thresholding modes.
simp_adj_adap.089	: test all three thresholding modes.
fifos_man.089	: tests the fifo pipe structure.
host_inter_man.089	: a relatively short file to test the host interface.

6. Concluding Remarks

Bimodal Thresholding:

To eliminate noise spikes, the pixel intensity is compared to an upper threshold value (Figure 28). If the intensity exceeds this value, then it is considered as noise and suppressed at the output.

Variable Frame Size:

The chip is capable of processing pixel frames with a variable size (number of rows and columns). This feature is useful in processing smaller frames faster.

Algorithm Enhancements:

As part of the adaptive thresholding algorithm, an intensity average for each pixel is computed (based on the 8 surrounding pixels). The average values for all the pixels of the same frame are summed and the result is made available to outside the chip, as a running sum average (Figure 29).

Appendix A. Block Diagrams, Schematics, and Timing Diagrams

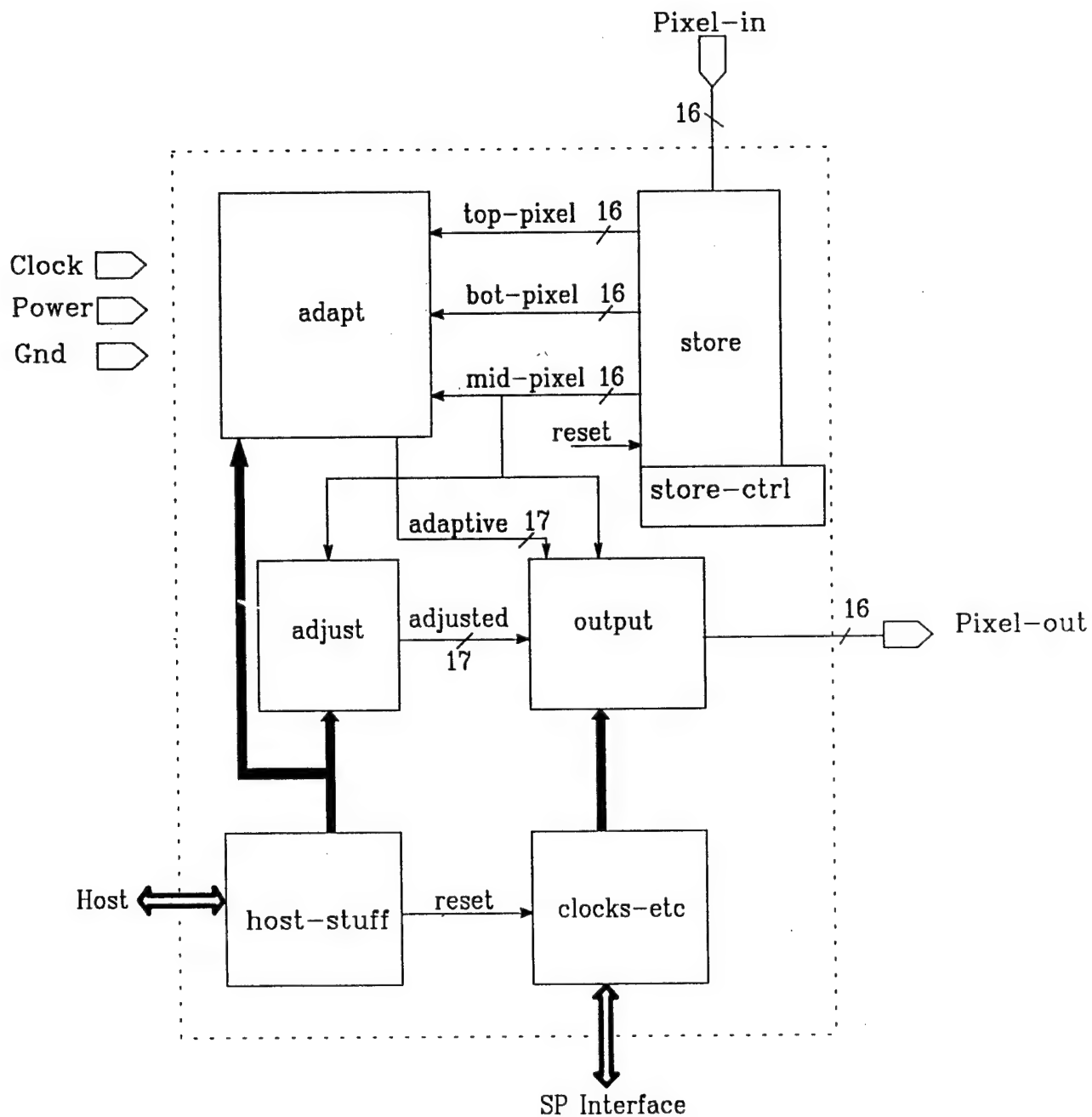


Figure 1. Thresholding Chip Block Diagram

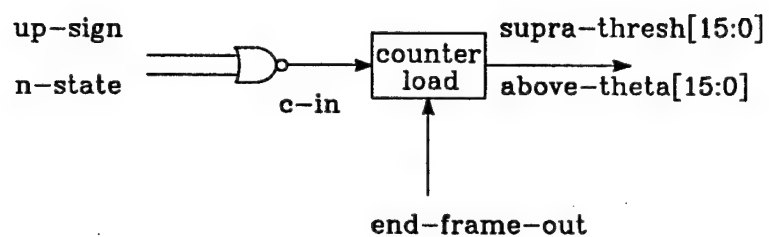


Figure 2. Counting of Pixels Above Threshold
(in output/mux1 block)

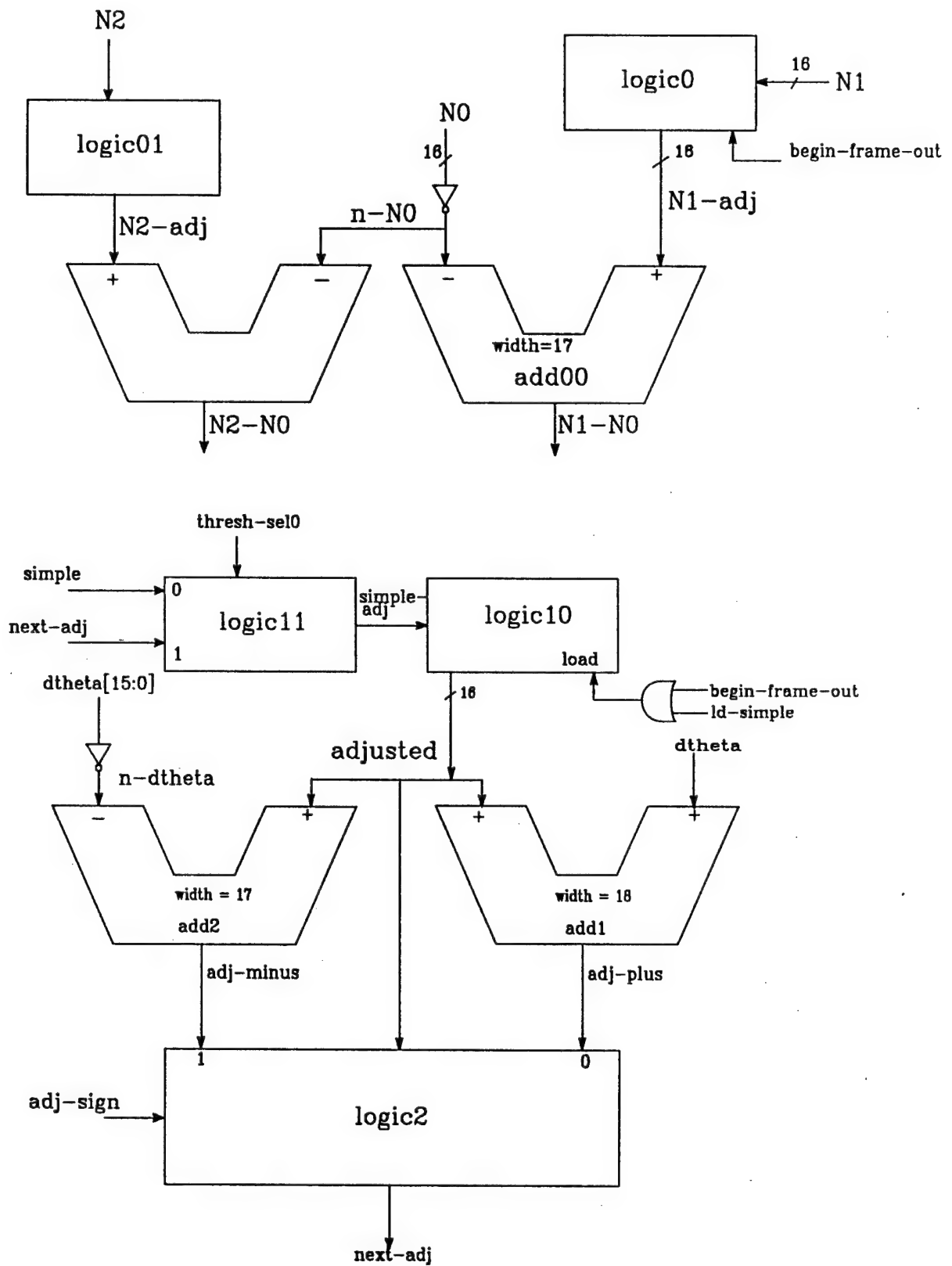


Figure 3. Simple-Adjust Threshold Hardware

adjust

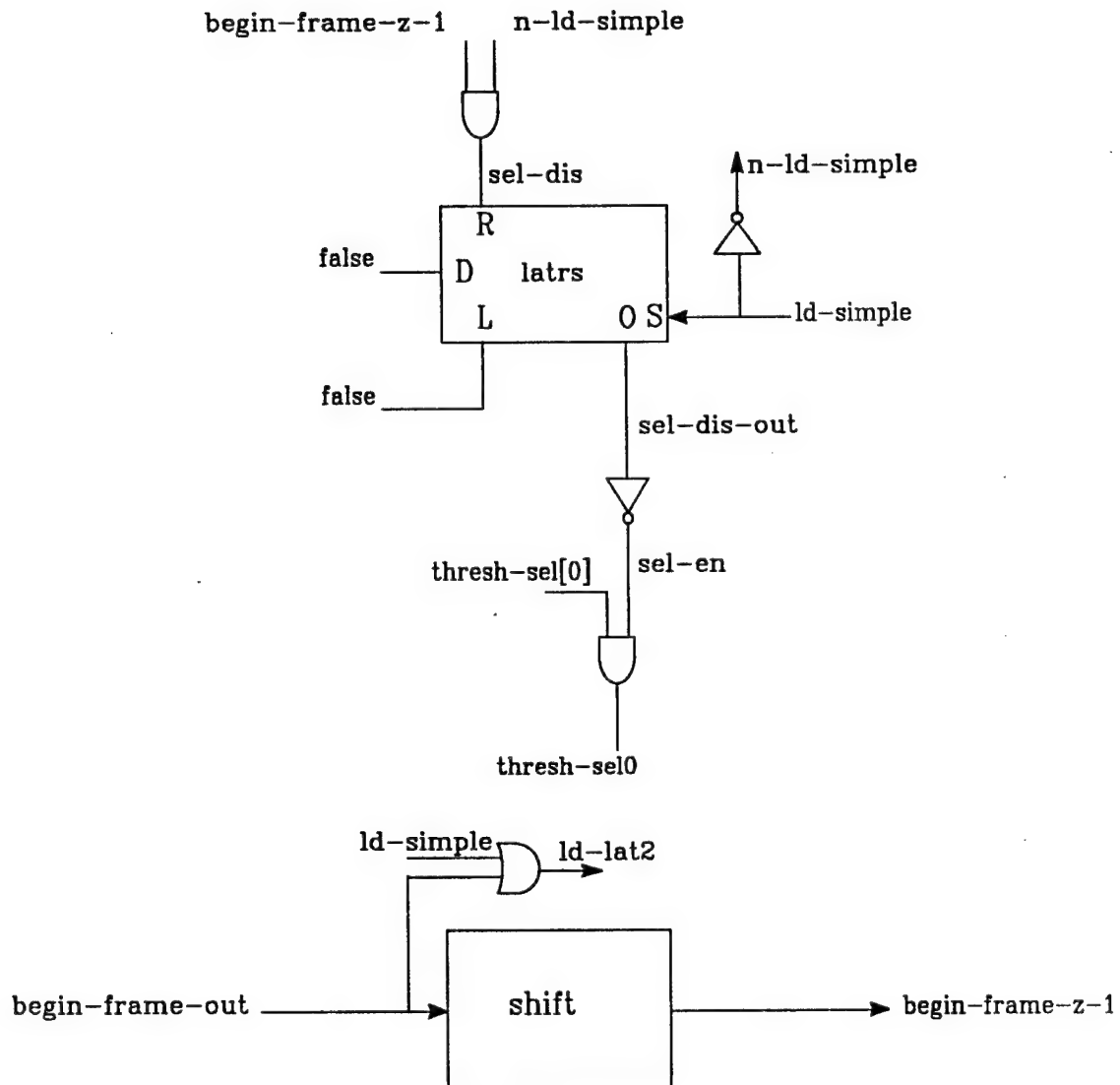


Figure 4. Adjust-Simple Threshold Selection
(in `adjust/logic3`)

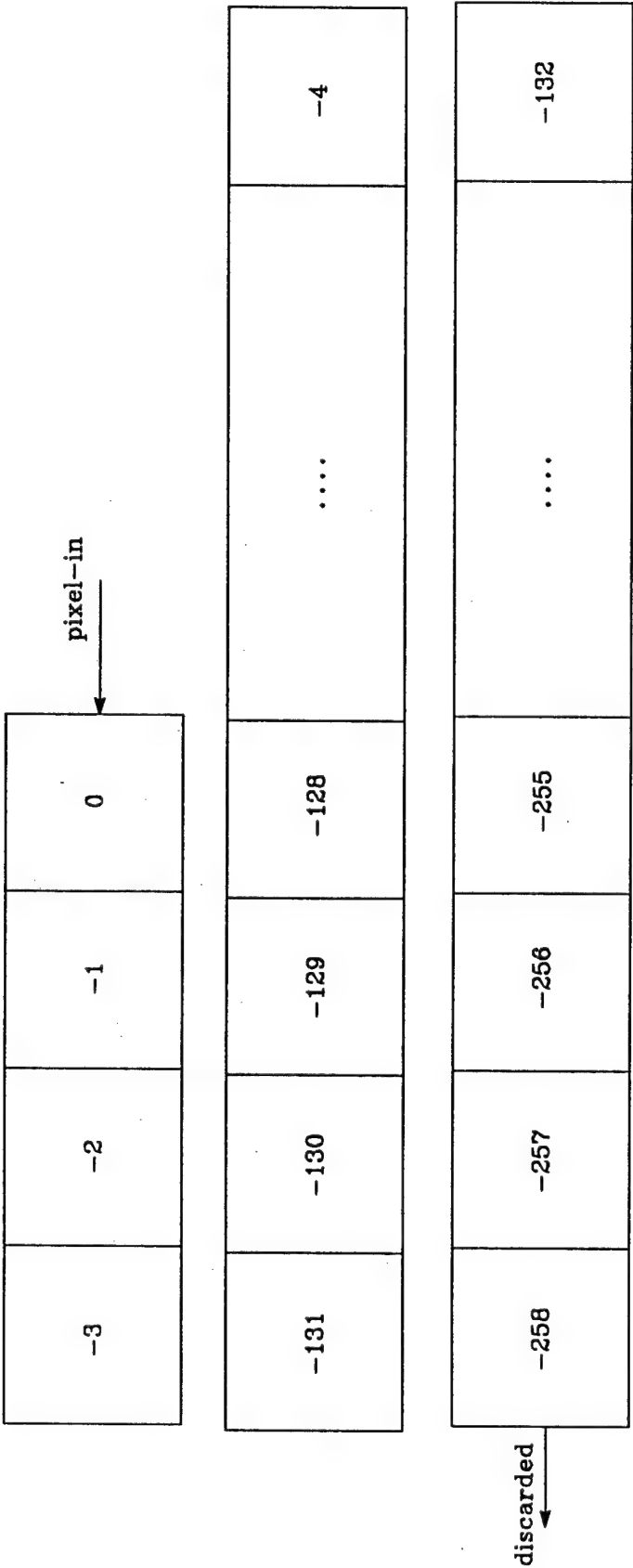


Figure 5. Pixel Stream Spatial Organization

$$S1 = XZ^{-3} + XZ^{-258}$$

$$S2 = S1 + XZ^{-131}$$

$$S3 = XZ^{-2} + XZ^{-257}$$

$$S4 = S3 + XZ^{-130}$$

$$S5 = XZ^{-1} + XZ^{-256}$$

$$S6 = S5 + XZ^{-129}$$

$$S7 = XZ^0 + XZ^{-255}$$

$$S8 = S7 + XZ^{-128}$$

$$S13 = XZ^1 + XZ^{-254}$$

$$S14 = S13 + XZ^{-127}$$

$$S15 = XZ^2 + XZ^{-253}$$

$$S16 = S15 + XZ^{-126}$$

$$S9 = S2 + S3$$

$$S10 = S9 + S6$$

$$S11 = S4 + S5$$

$$S12 = S11 + S8$$

$$S17 = S6 + S7$$

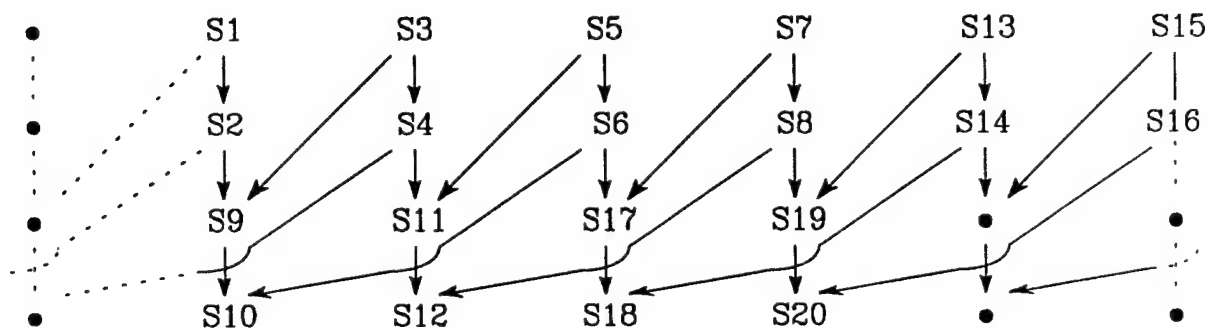
$$S18 = S17 + S14$$

$$S19 = S8 + S13$$

$$S20 = S19 + S16$$

ETC

(a)



(b)

Figure 6. Chart of Arithmetic Operations

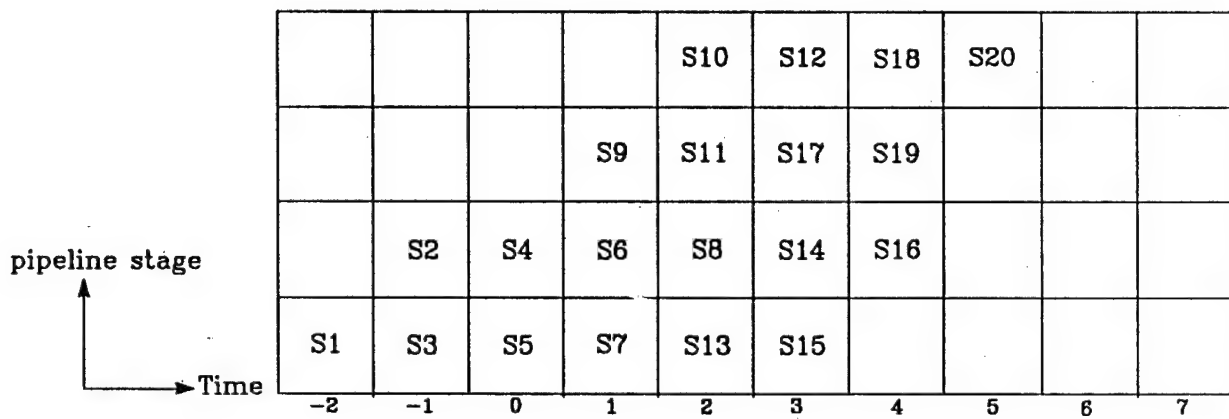


Figure 7. Pipeline Reservation Table

$$\theta = K1.E(X) + K2.L1 + K3 \quad E(X) = \frac{\sum X_i}{8} = \bar{X} \quad L1 = \sum |X_i - \bar{X}| \quad i = 0,1,2,3,4,5,6,7$$

X2	X1	X0
X4		X3
X7	X6	X5

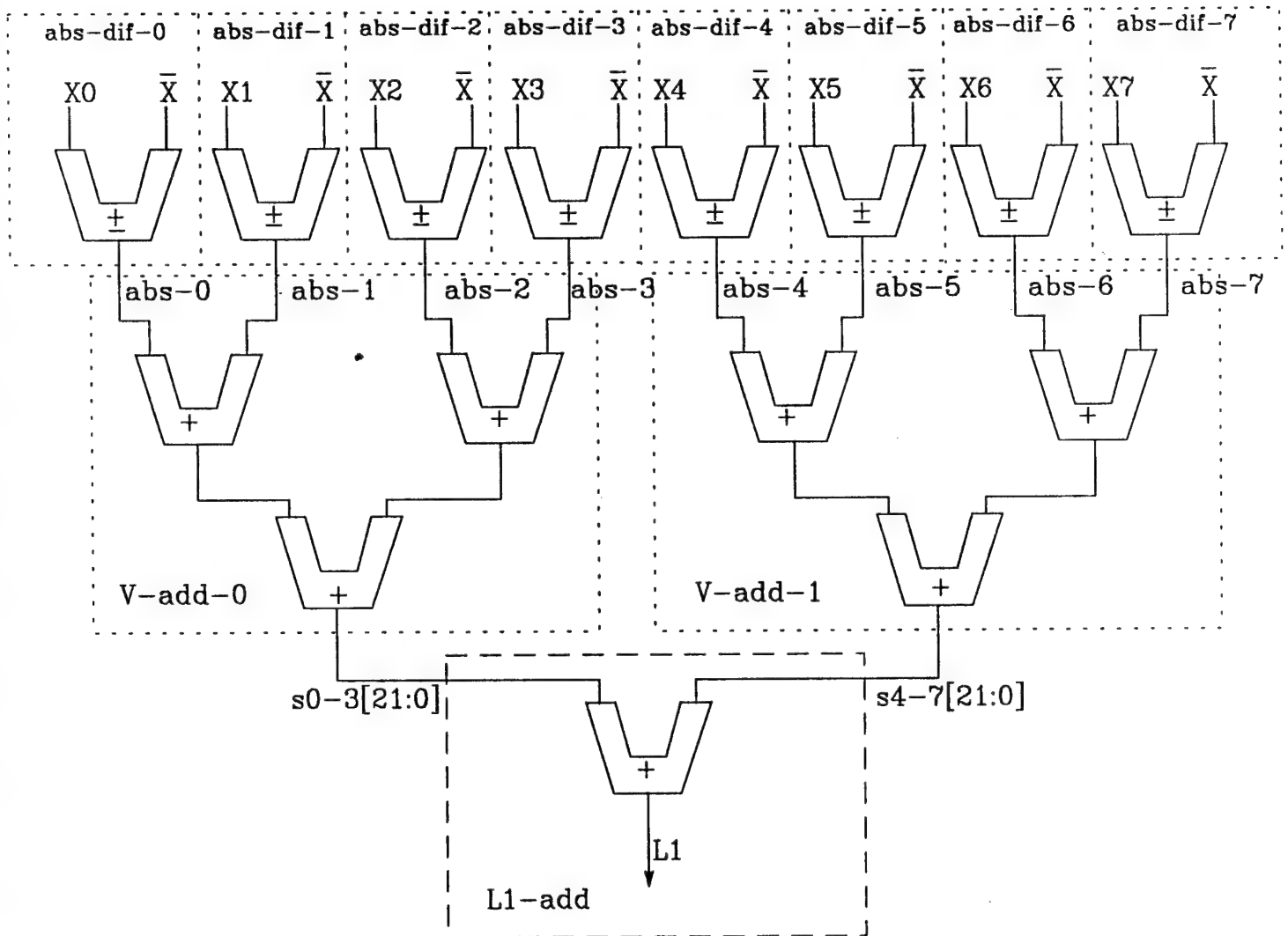


Figure 8. L1 Norm Computation

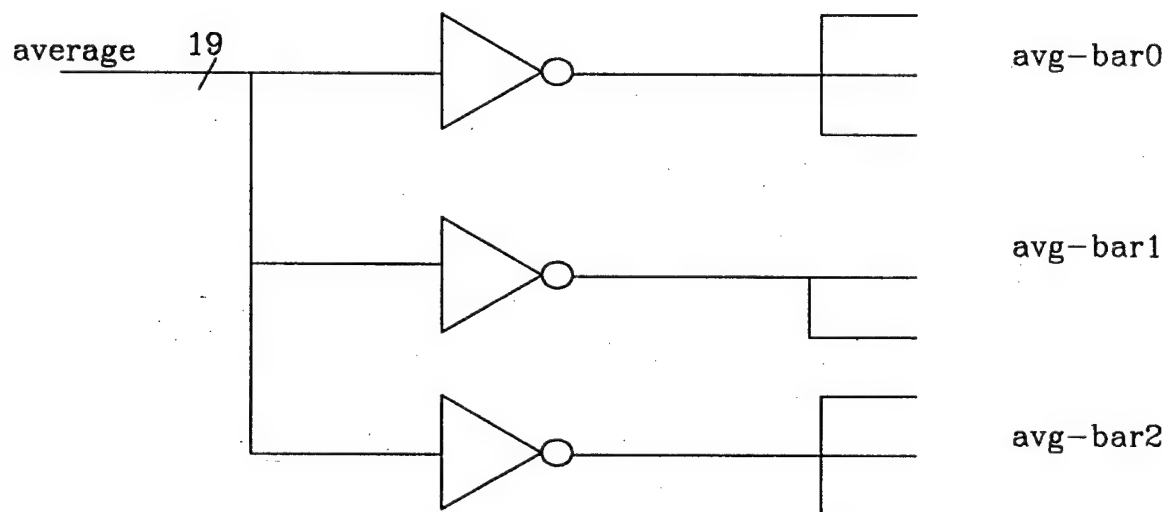


Figure 9. Inverting Buffer Tree Structure For Average

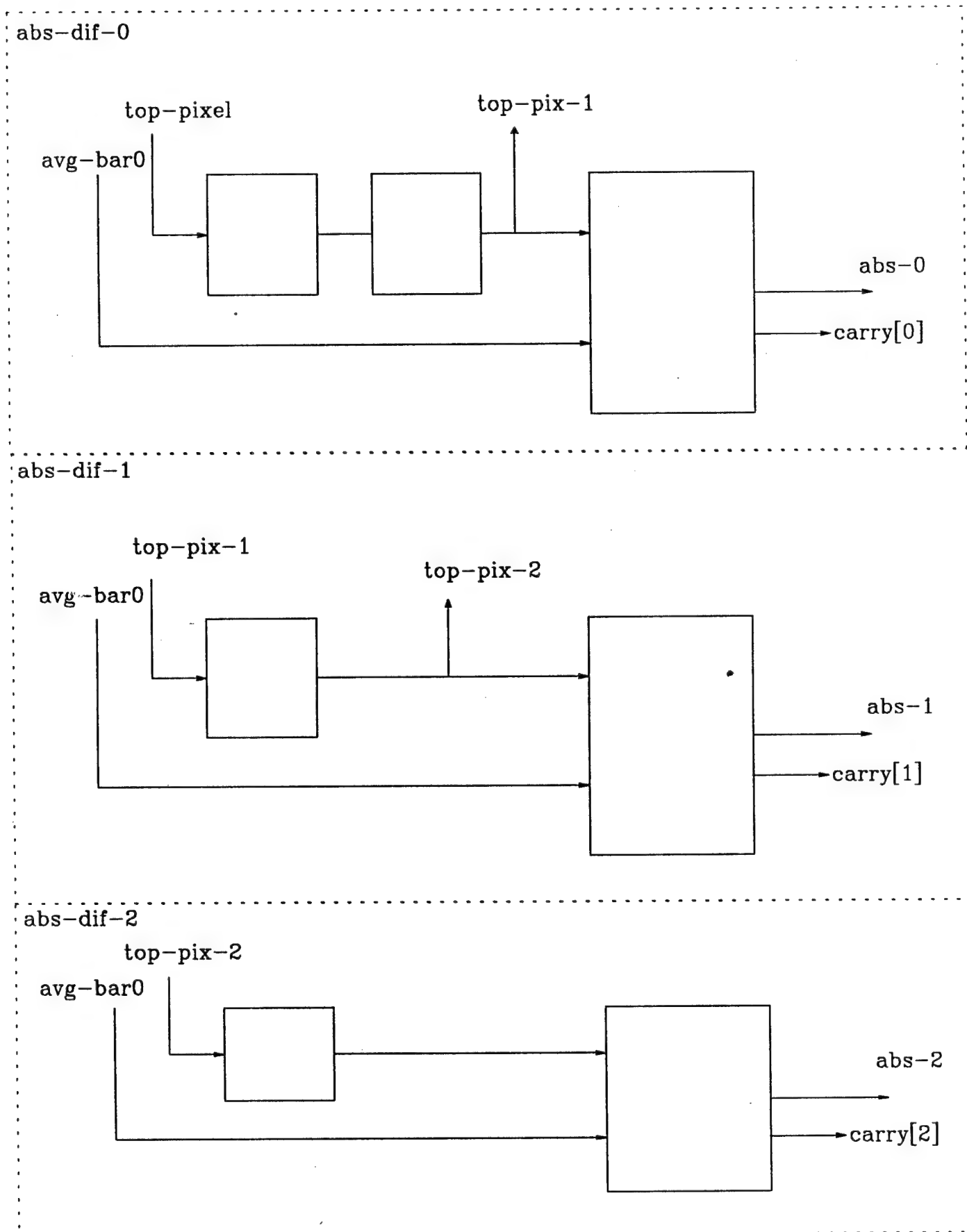


Figure 10. Details of L1 Norm Hardware (1 of 6).

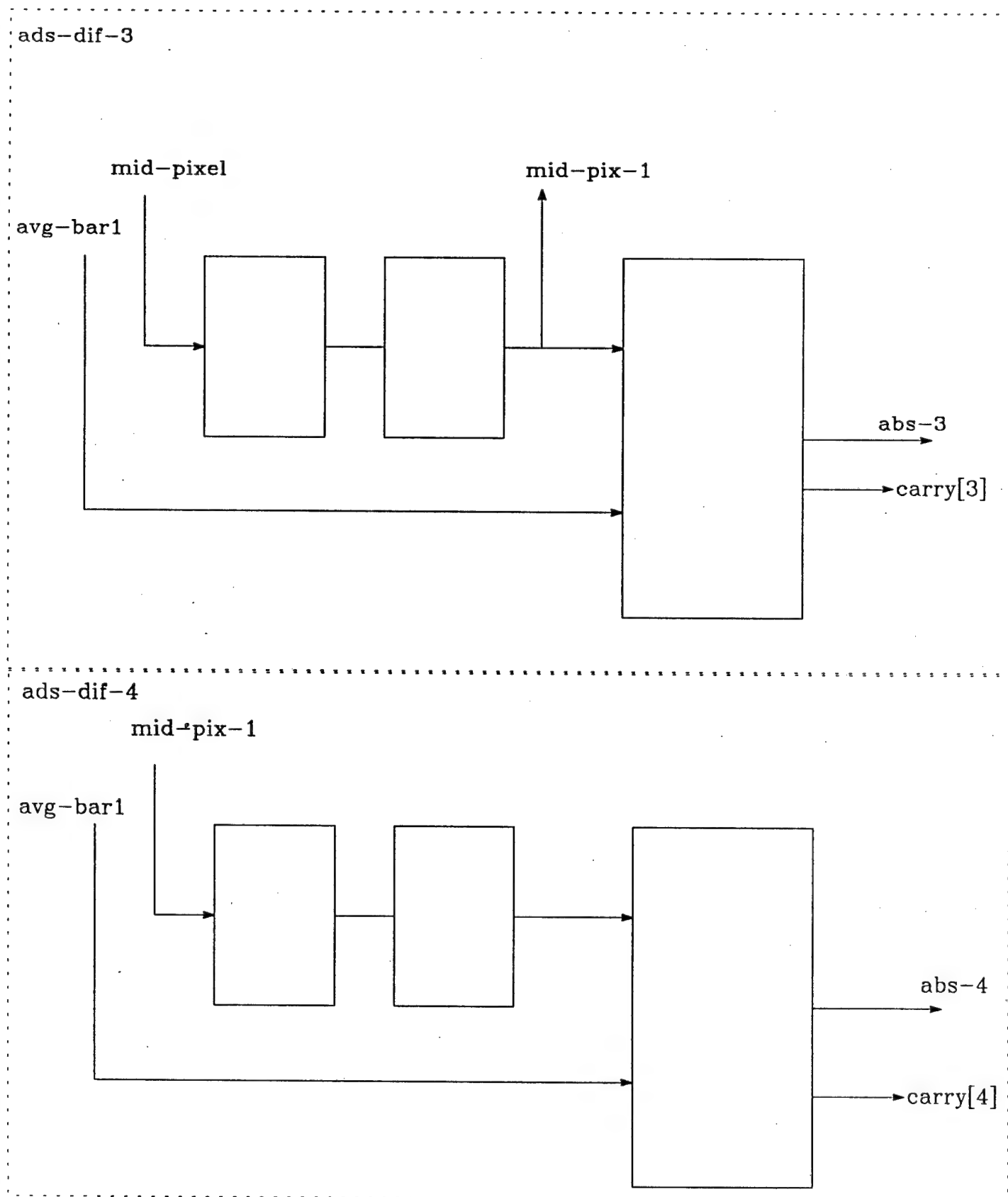


Figure 10. Details of L1 Norm Hardware (2 of 6).

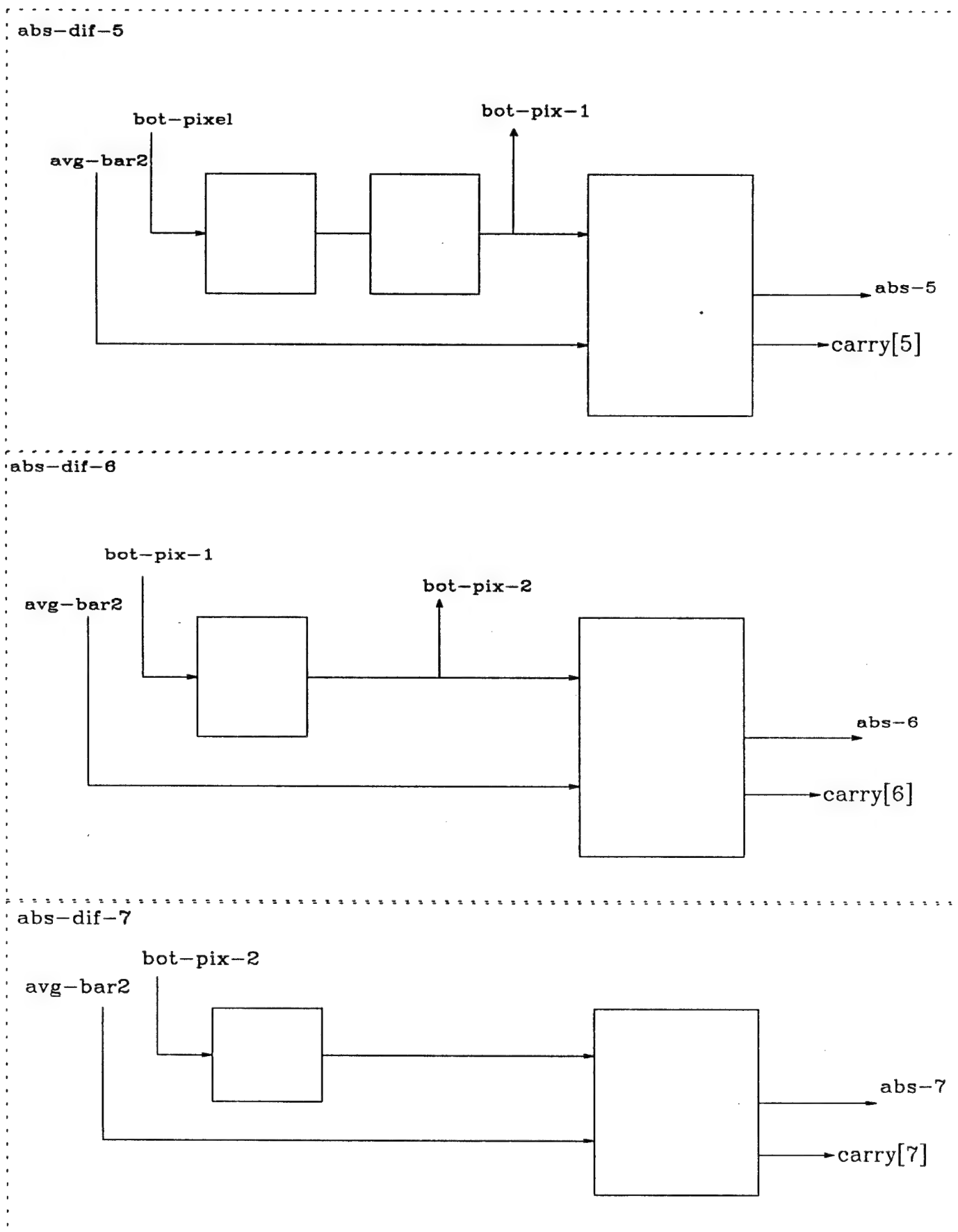


Figure 10. Details of L1 Norm Hardware (3 of 6).

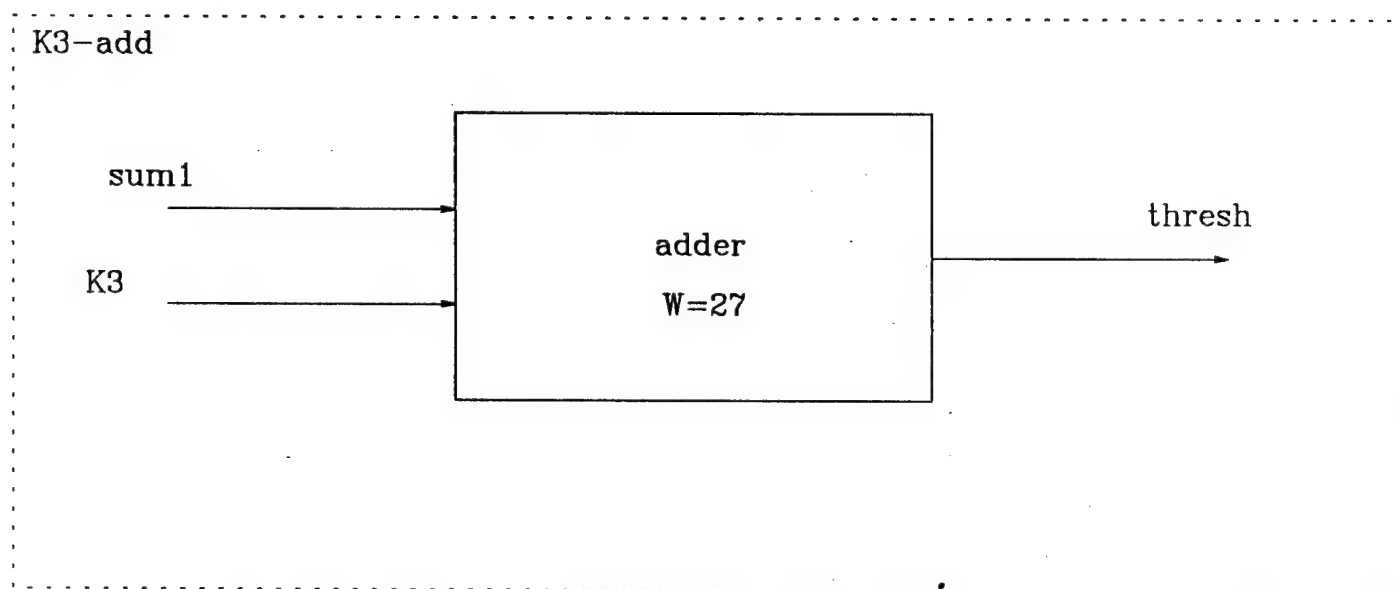


Figure 10. Details of L1 Norm Hardware (4 of 6).

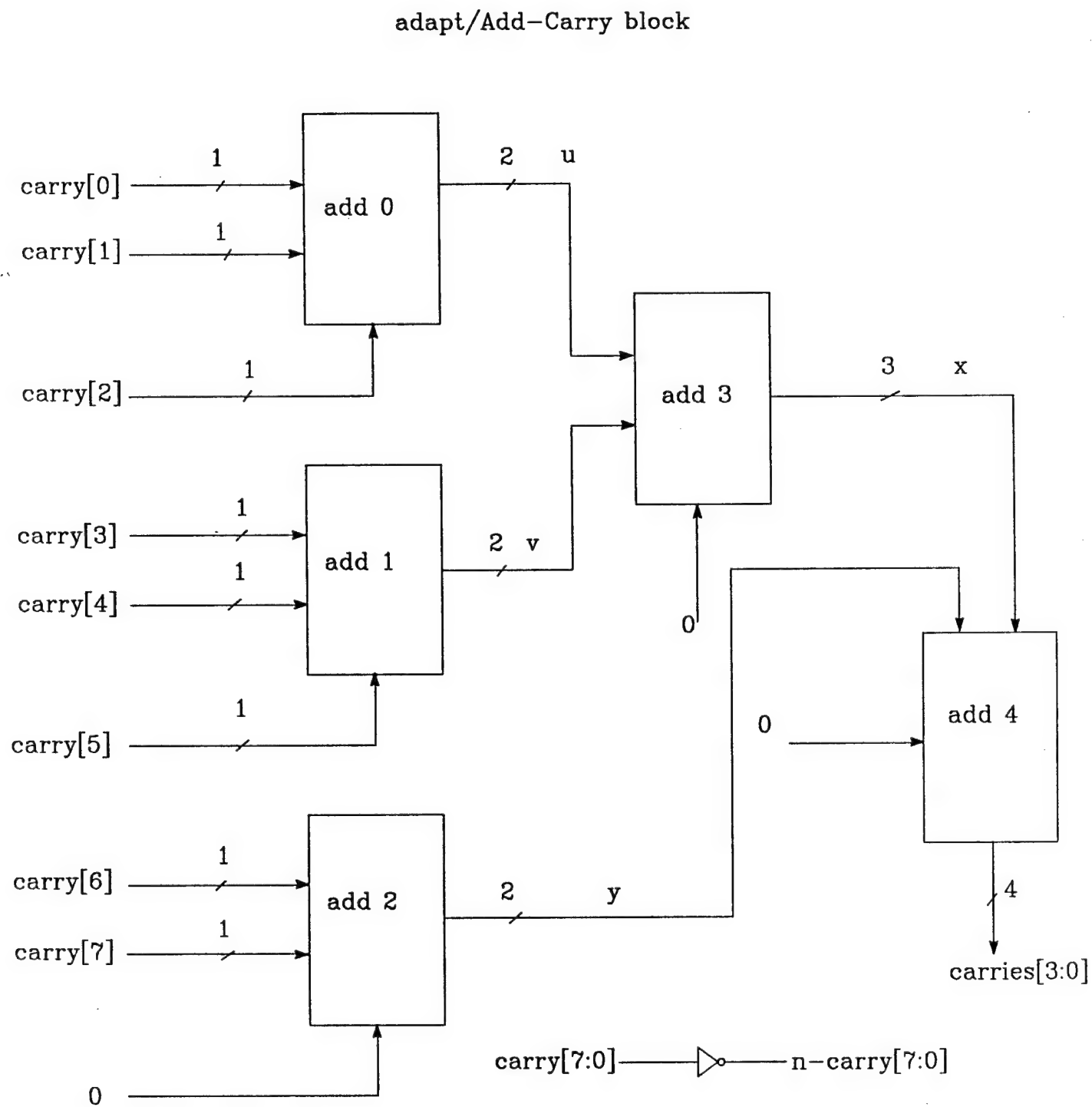


Figure 10. Details of L1 Norm Hardware (5 of 6).

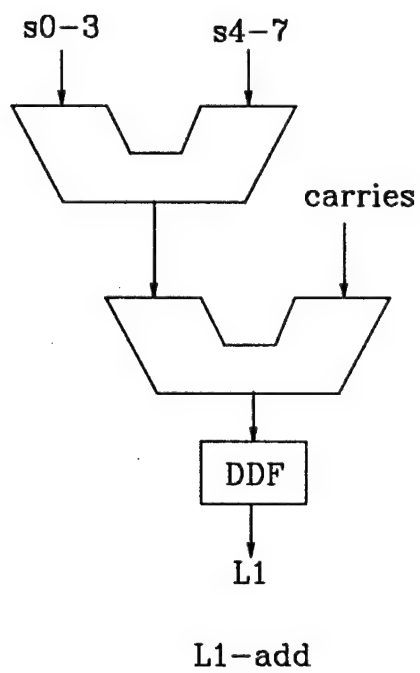


Figure 10. Details of L1 Norm Hardware (6 of 6).

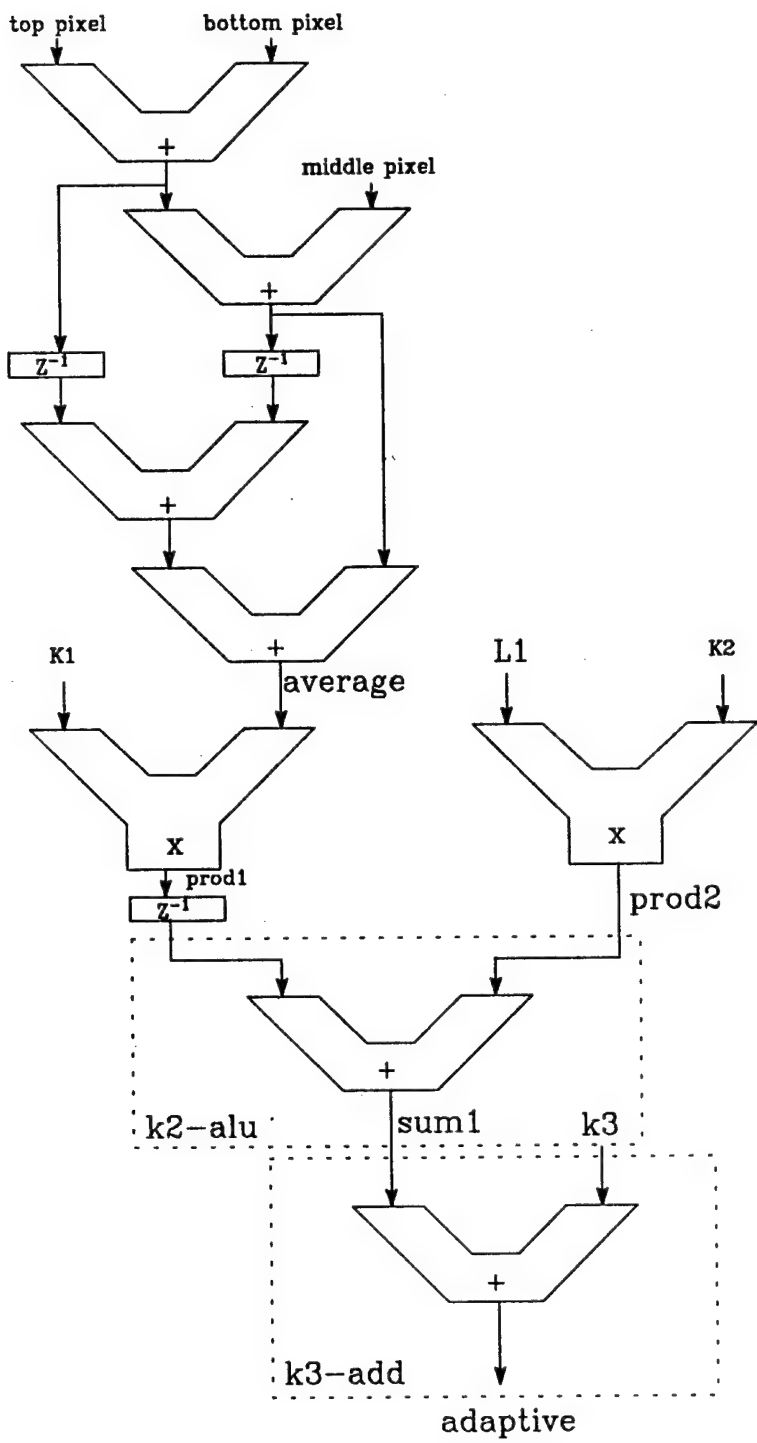
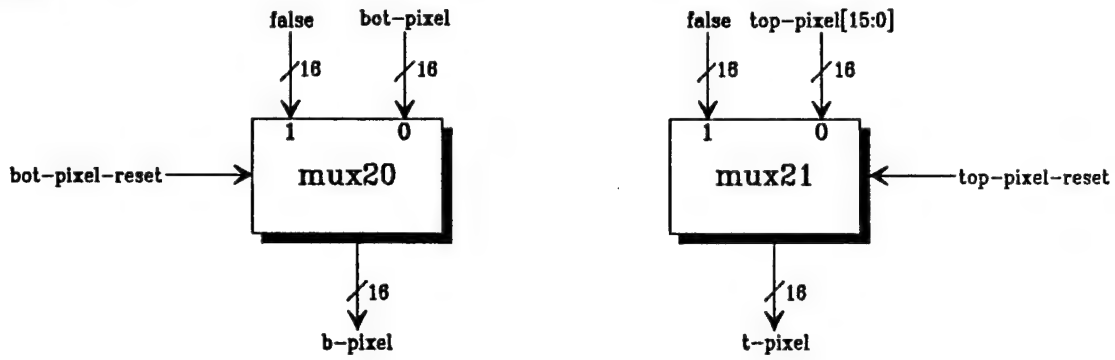
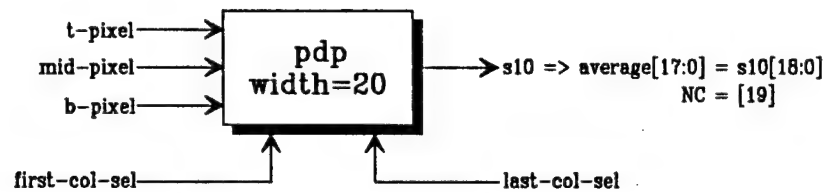


Figure 11. Adaptive Threshold Hardware

muxes

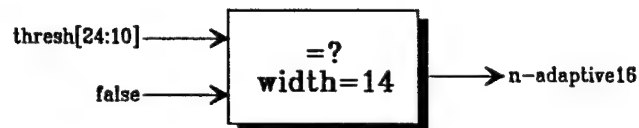


A0-3



MSTflag

thresh[34:0] = NC, thresh[33:20], adaptive[15:0], NC*4



k1-add

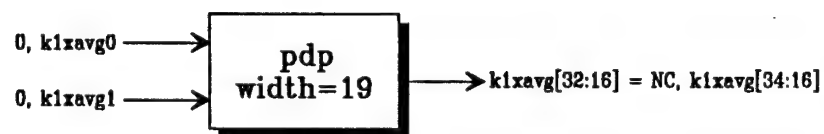
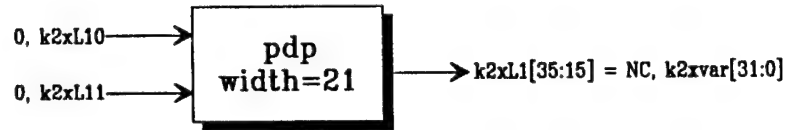


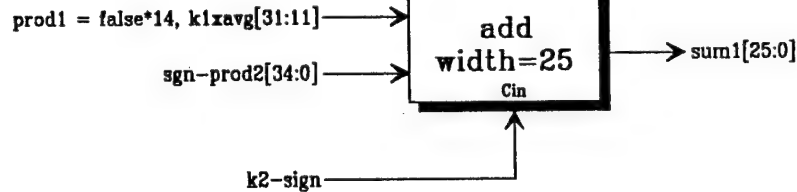
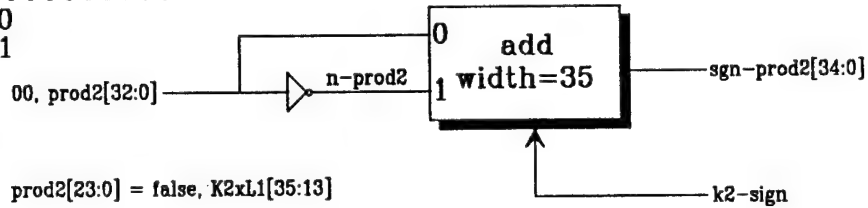
Figure 12. Adaptive Threshold Computation (1/3)

k2-add

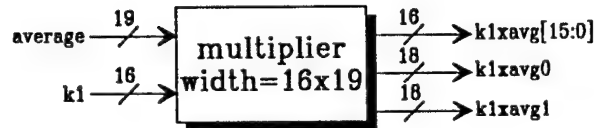
k2xvar[45:0] = NC, prod2[32:0], NC*12



k2-alu

k2-ctrl0
k2-ctrl1

mult-k1



mult-k2

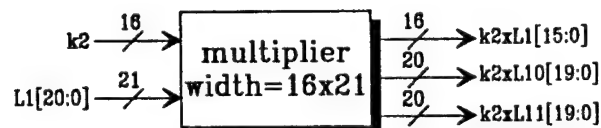
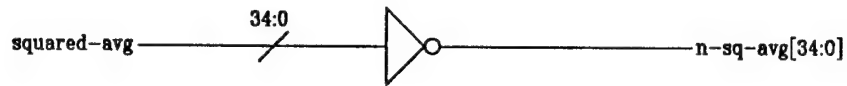
k2xL1[14:13] = prod2[1:0]
k2xL1[37:16] = prod2[23:2]

Figure 12. Adaptive Threshold Computation (2/3)

var-inv0 : invert 0 - 15
var-inv1 : invert 16 - 34



var-inv0
var-inv1

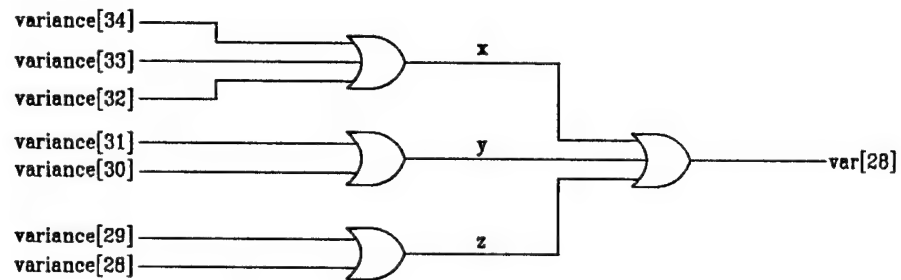
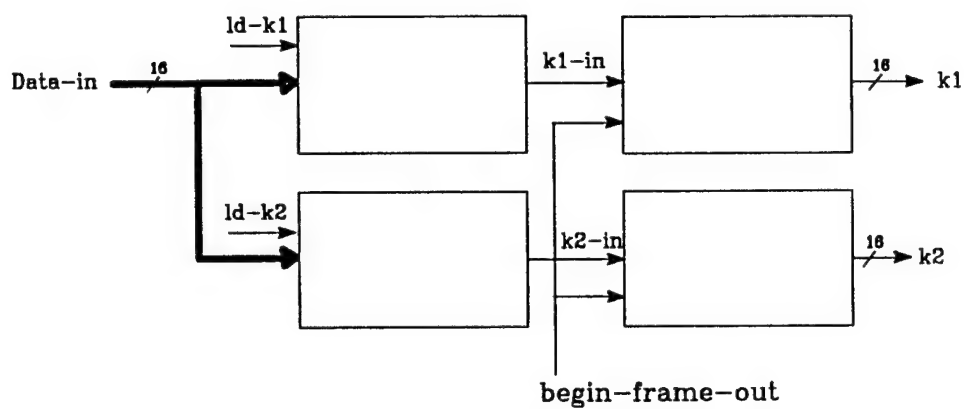
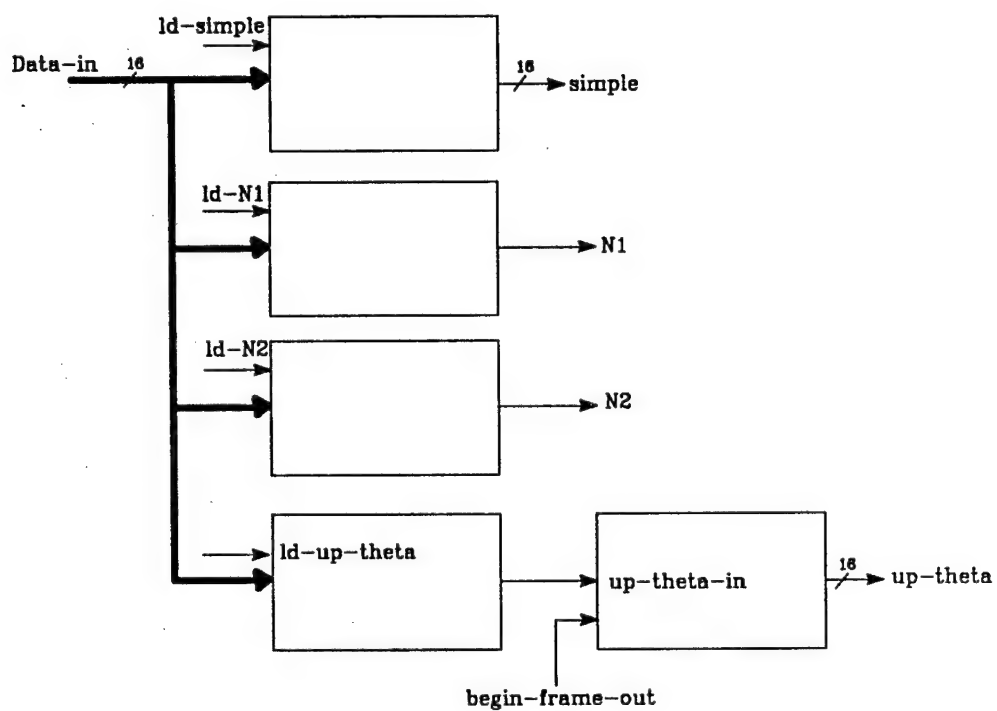


Figure 12. Adaptive Threshold Computation (3/3)

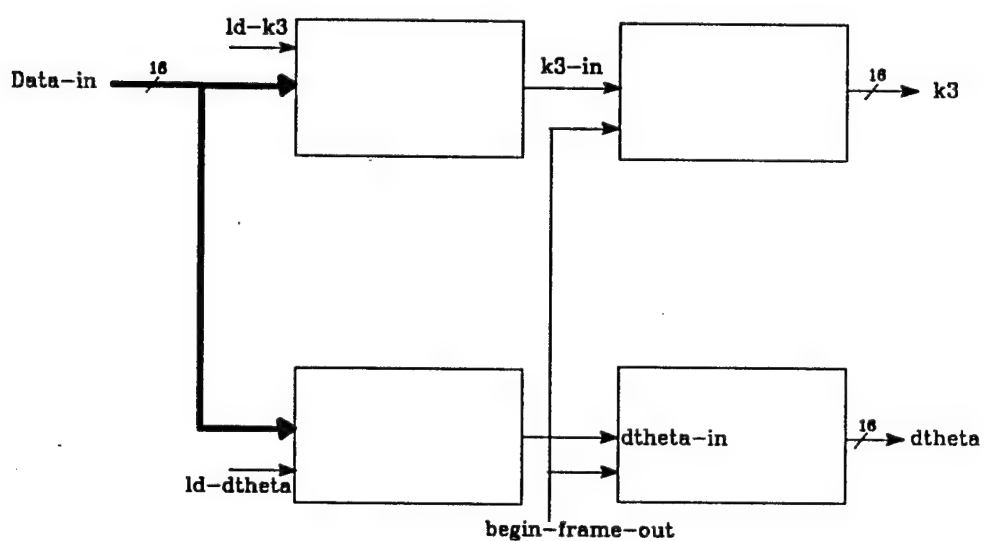


(a). reg0 Block



(b). reg1 Block

Figure 13. Host interface Module Block Diagram



(c). reg2 Block

Figure 13. Host Interface Module Block Diagram
(Continued)

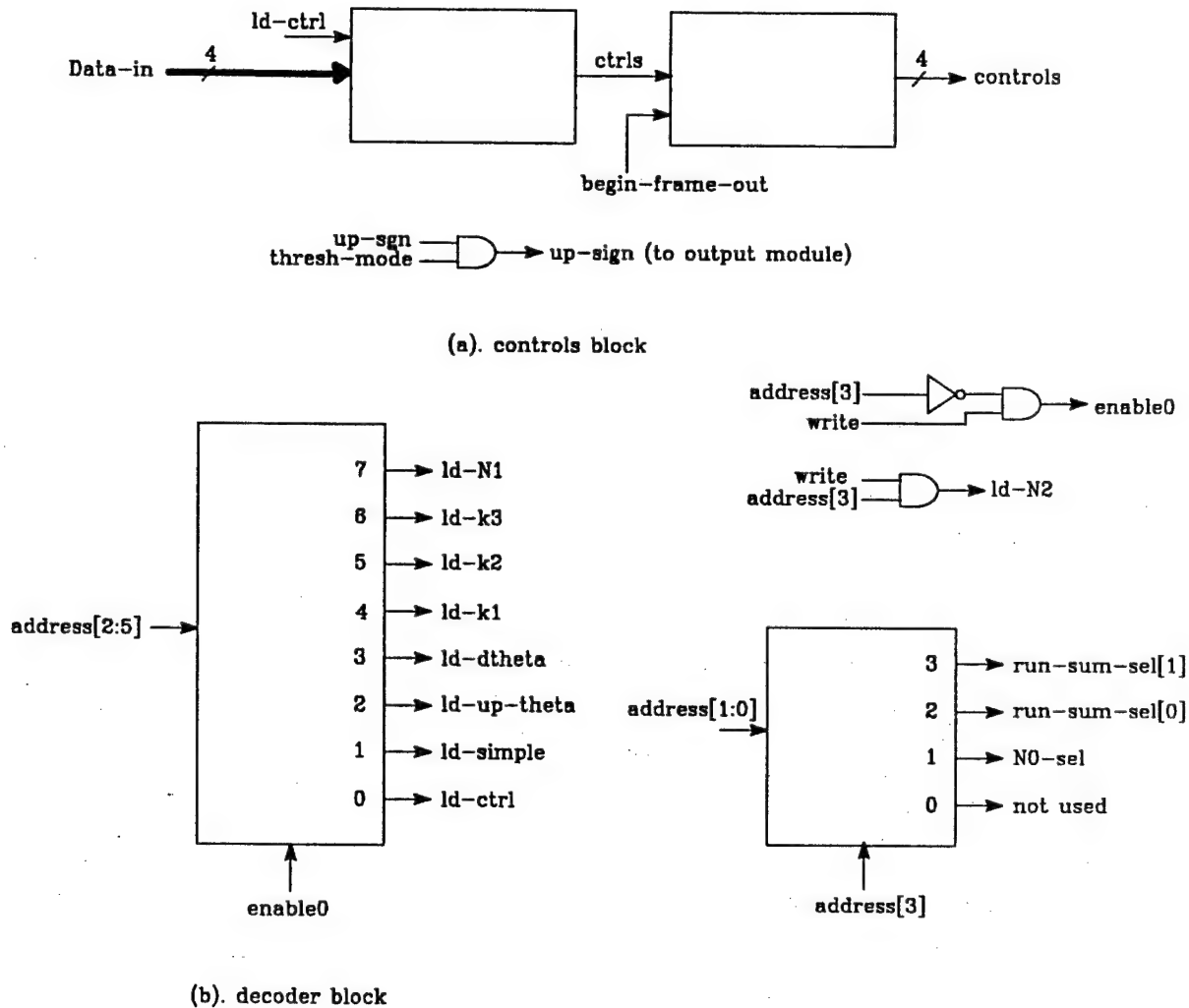


Figure 14. Host Interface Block Diagram (continued)

Table 1. Control Bits Assignment

controls[0]	unused
controls[2:1]	thresh-sel[1:0]
controls[3]	thresh-mode (0: mono, 1: bi-modal)

Table2. Threshold Selection

thresh-sel [1:0]	threshold type
00	simple
01	adjusted
10	adaptive
11	unused

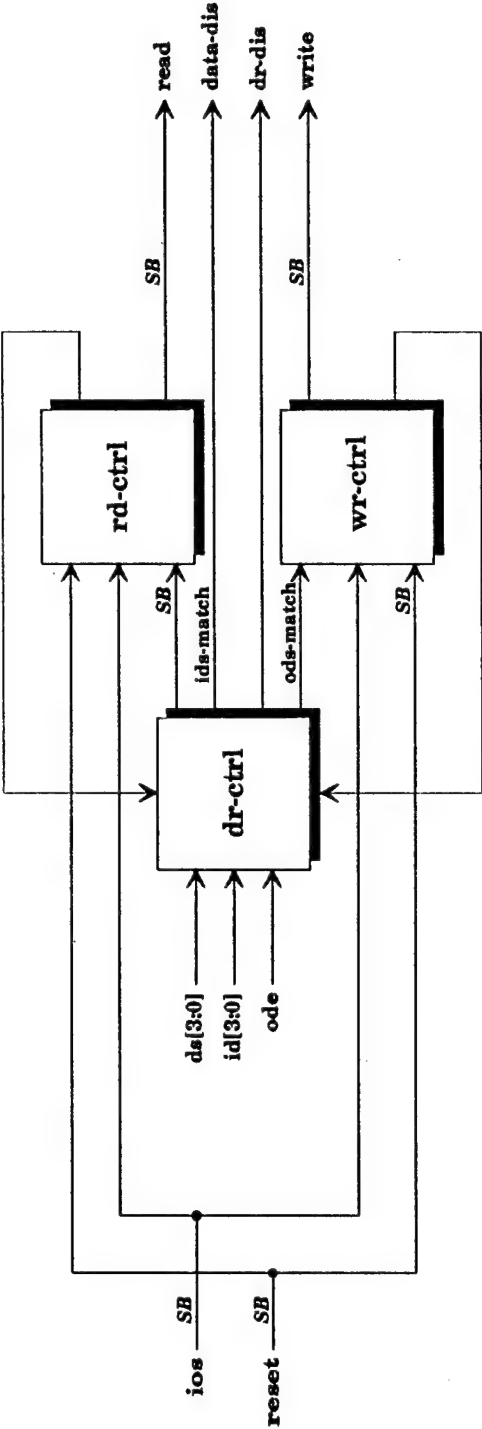


Figure 15. Host Interface Block Diagram

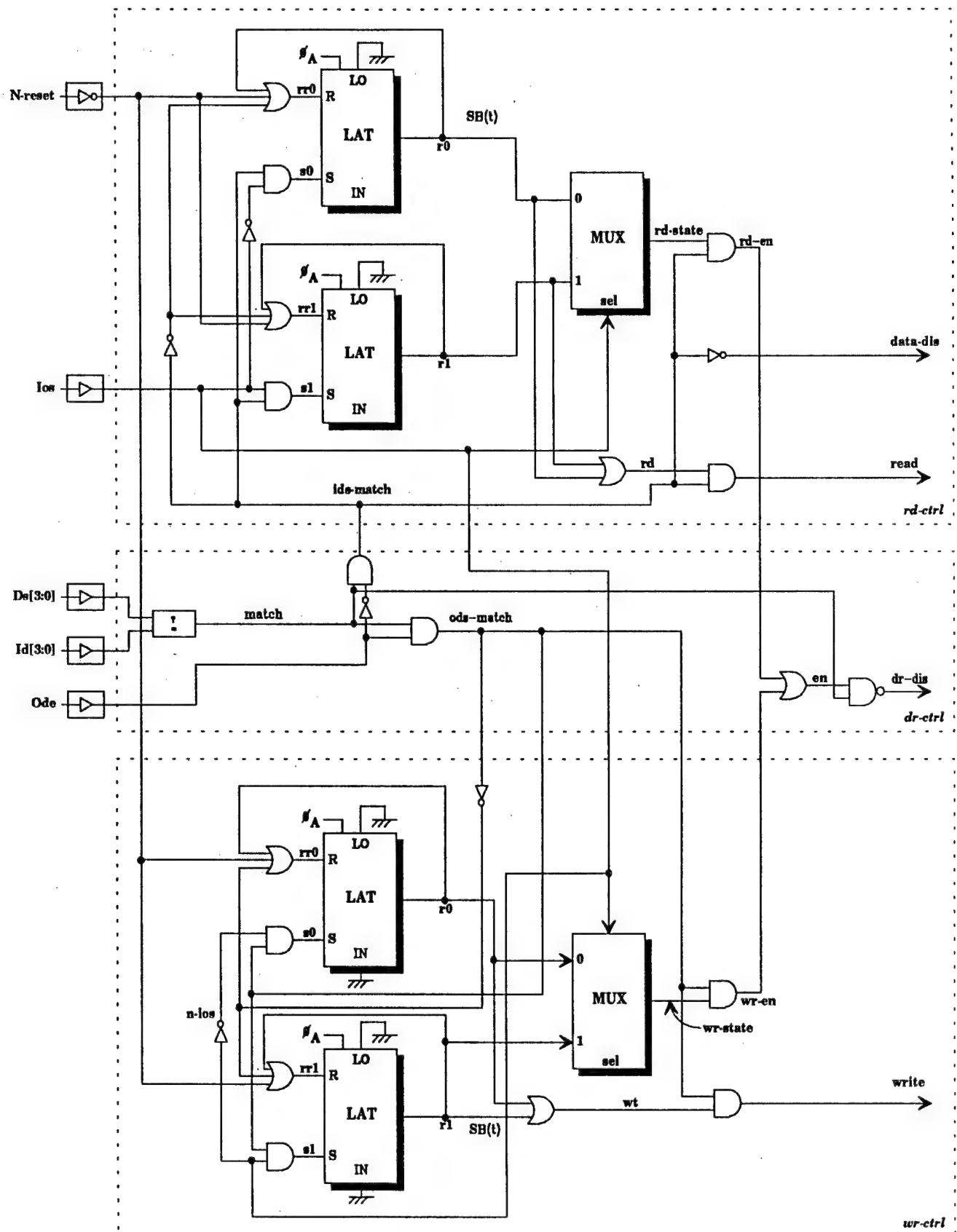


Figure 16. Host-stuff/interface module

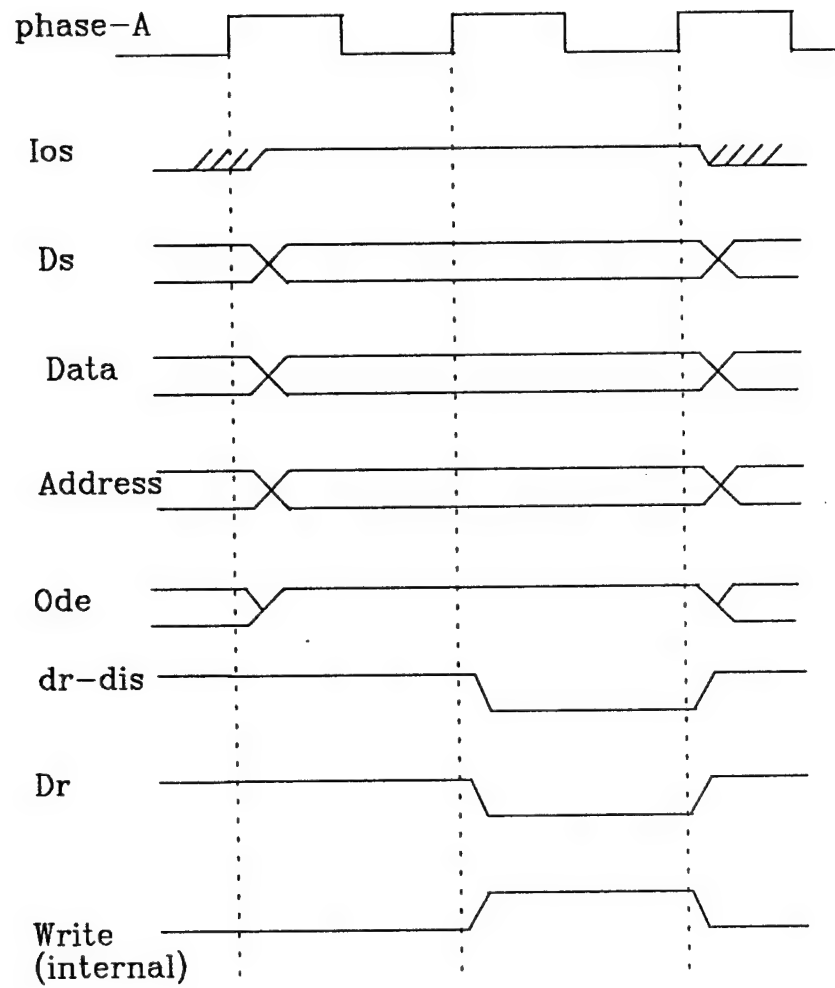


Figure 17. Host Interface Timing (write cycle)

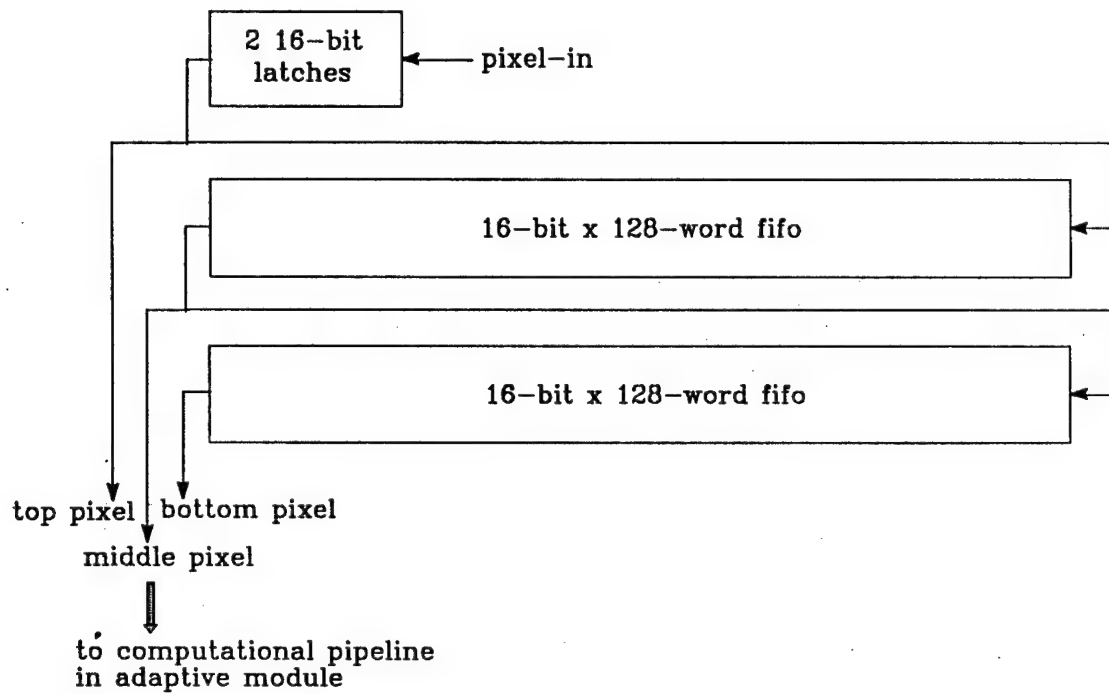


Figure 18. Main Storage Organization and Control

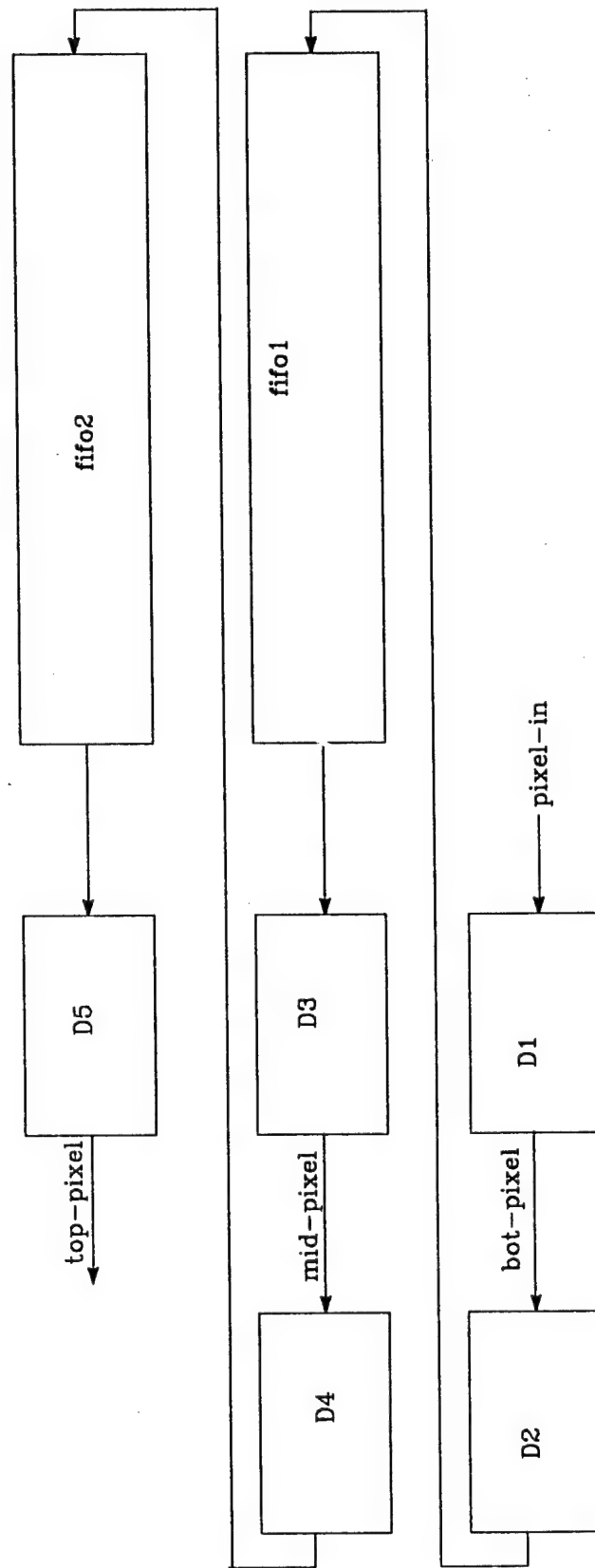


Figure 19. Schematic of Fifos Pipe Structure
(Imported From GT-VSF Chip).

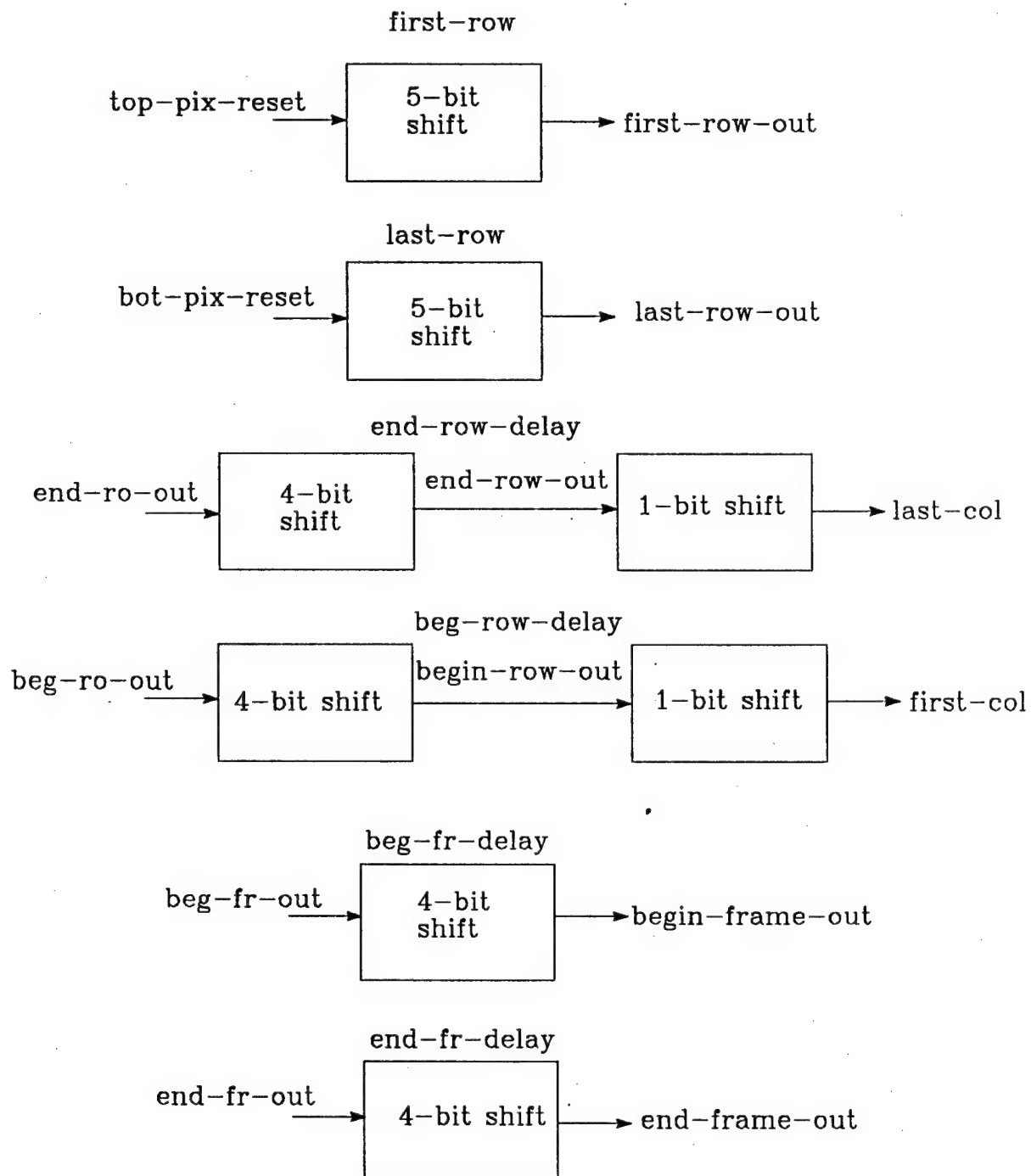


Figure 20. Blocks in clocks-etc Module.

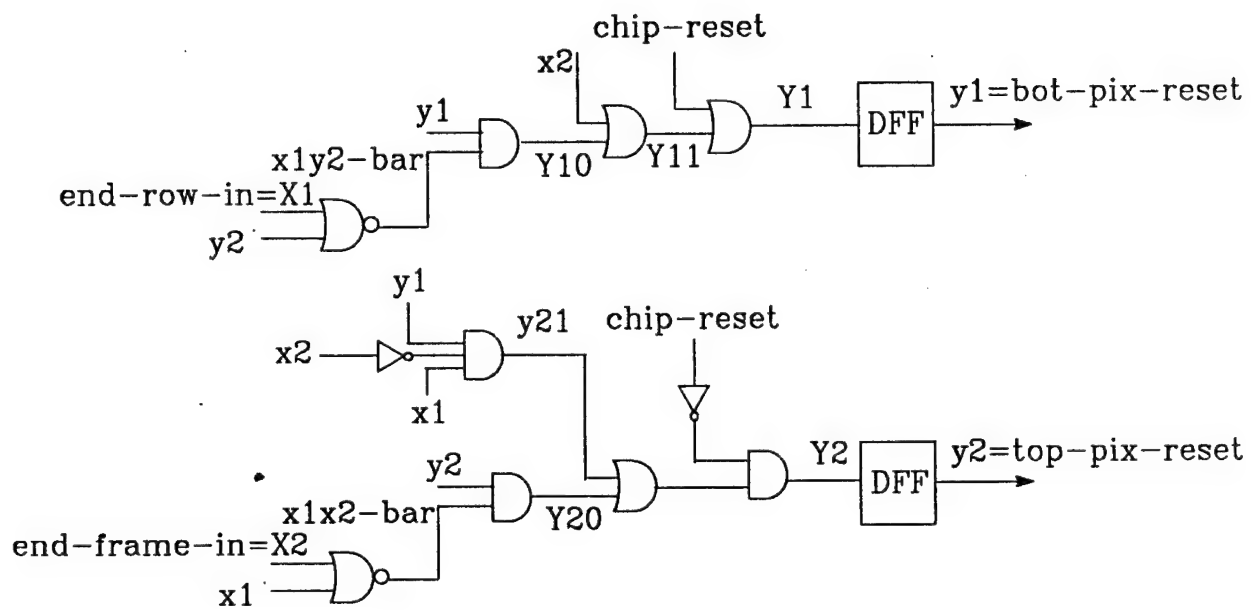
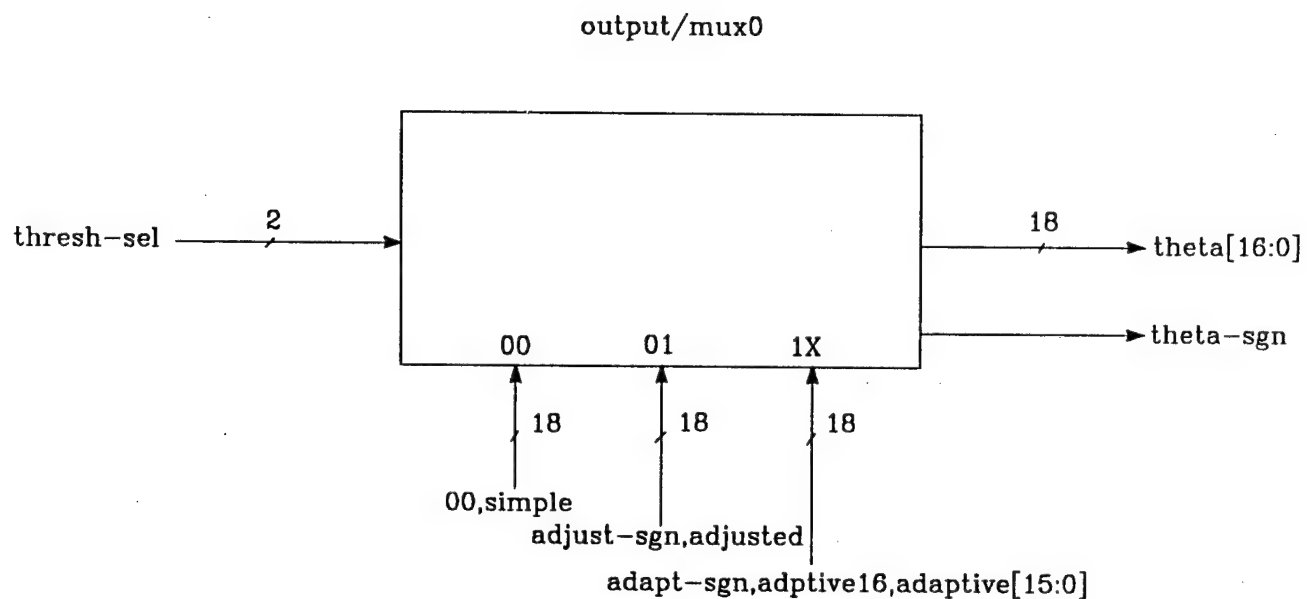
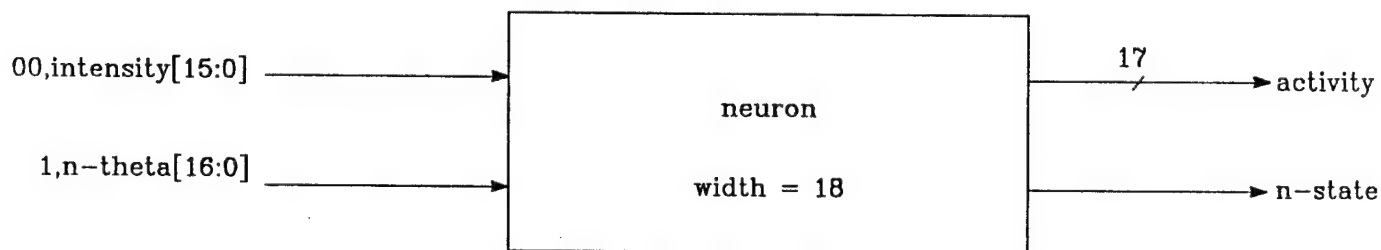


Figure 21. clocks-etc/state-mach Block Diagram.



(a) Threshold Selection



(b) Low Threshold Operation

Figure 22. Thresholding Operation

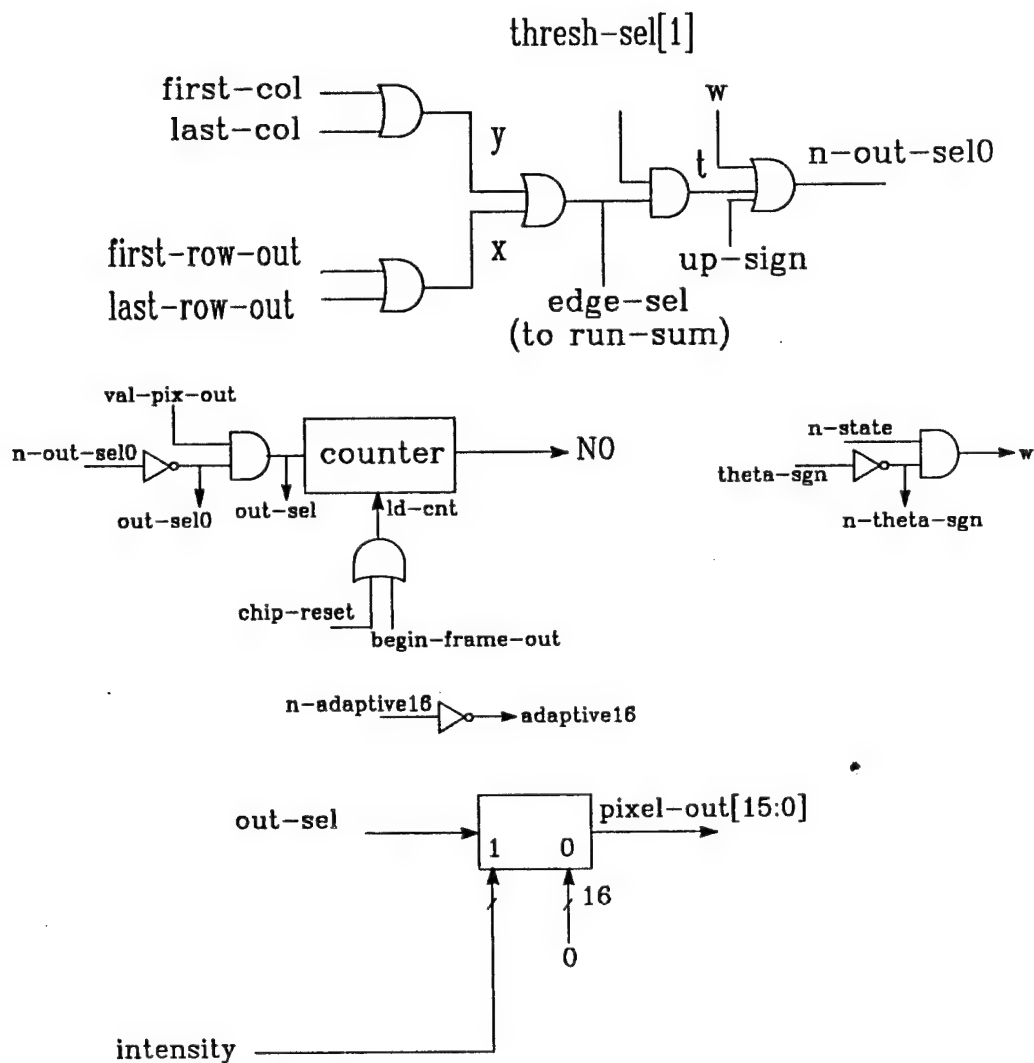


Figure 23. Output Selection Logic
(output/mux1 block)

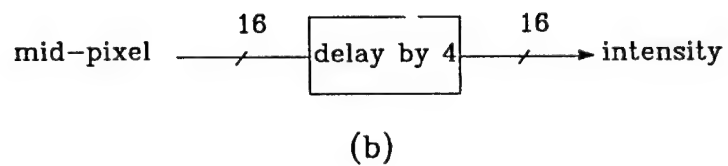
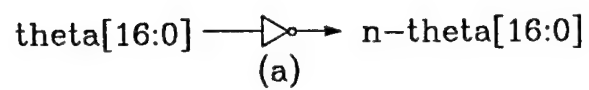


Figure 24. invert and delay Blocks in Output Module

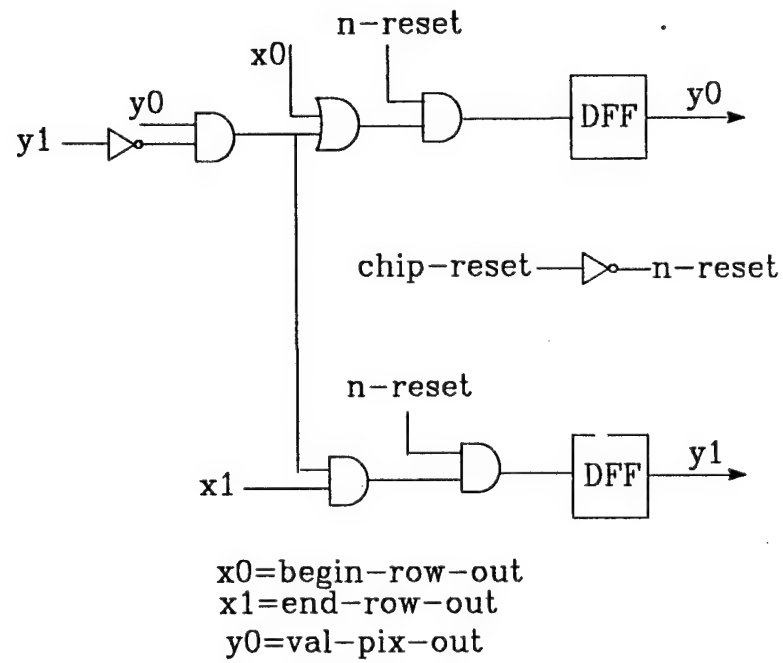


Figure 25. output/state-mach Block Diagram.

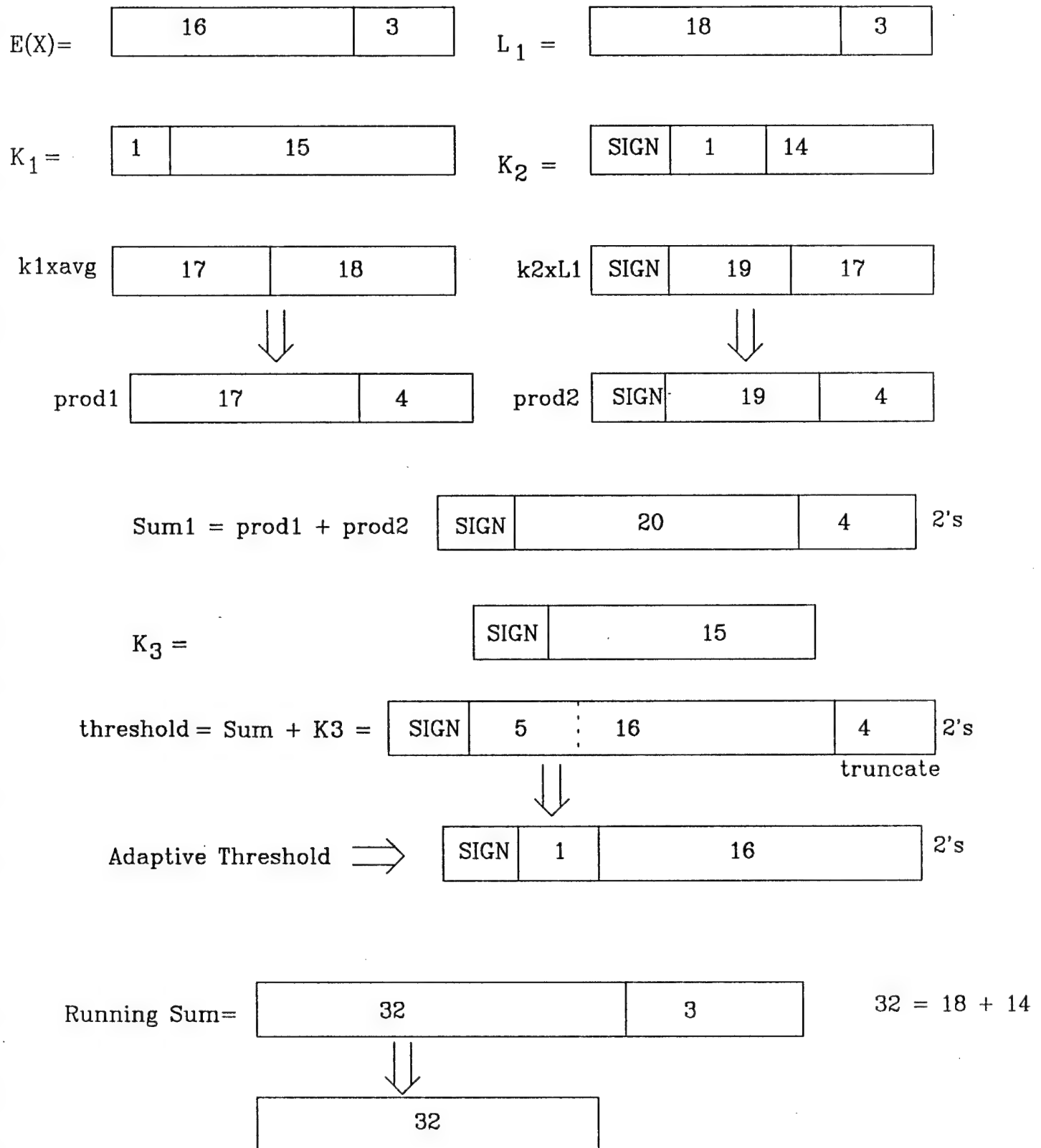


Figure 26. Truncation Scheme for Adaptive Thresholding

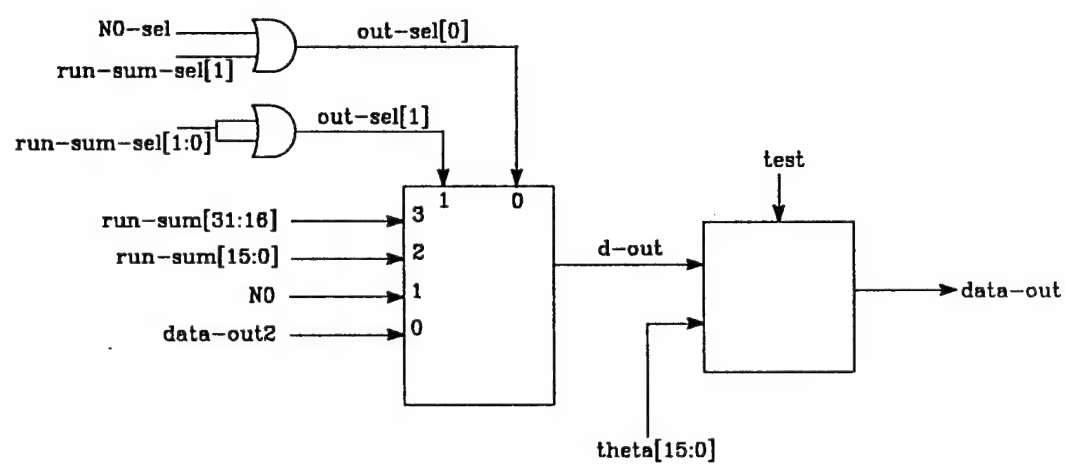


Figure 27. host-stuff/d-out-mux Block Diagram.

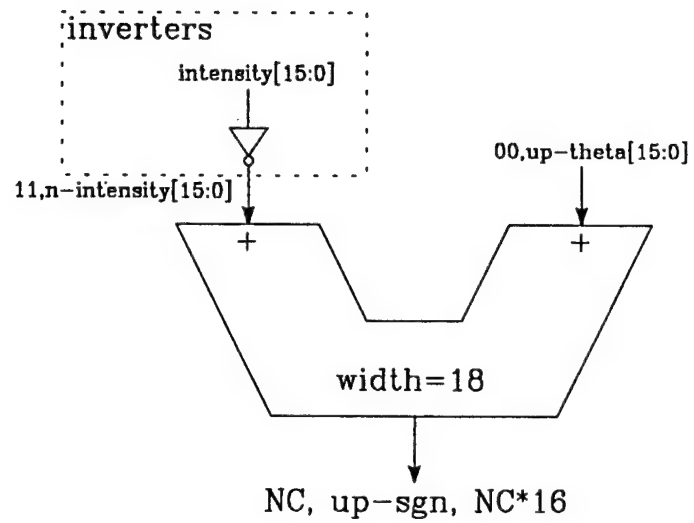


Figure 28. Upper threshold mode
(in host-stuff module)

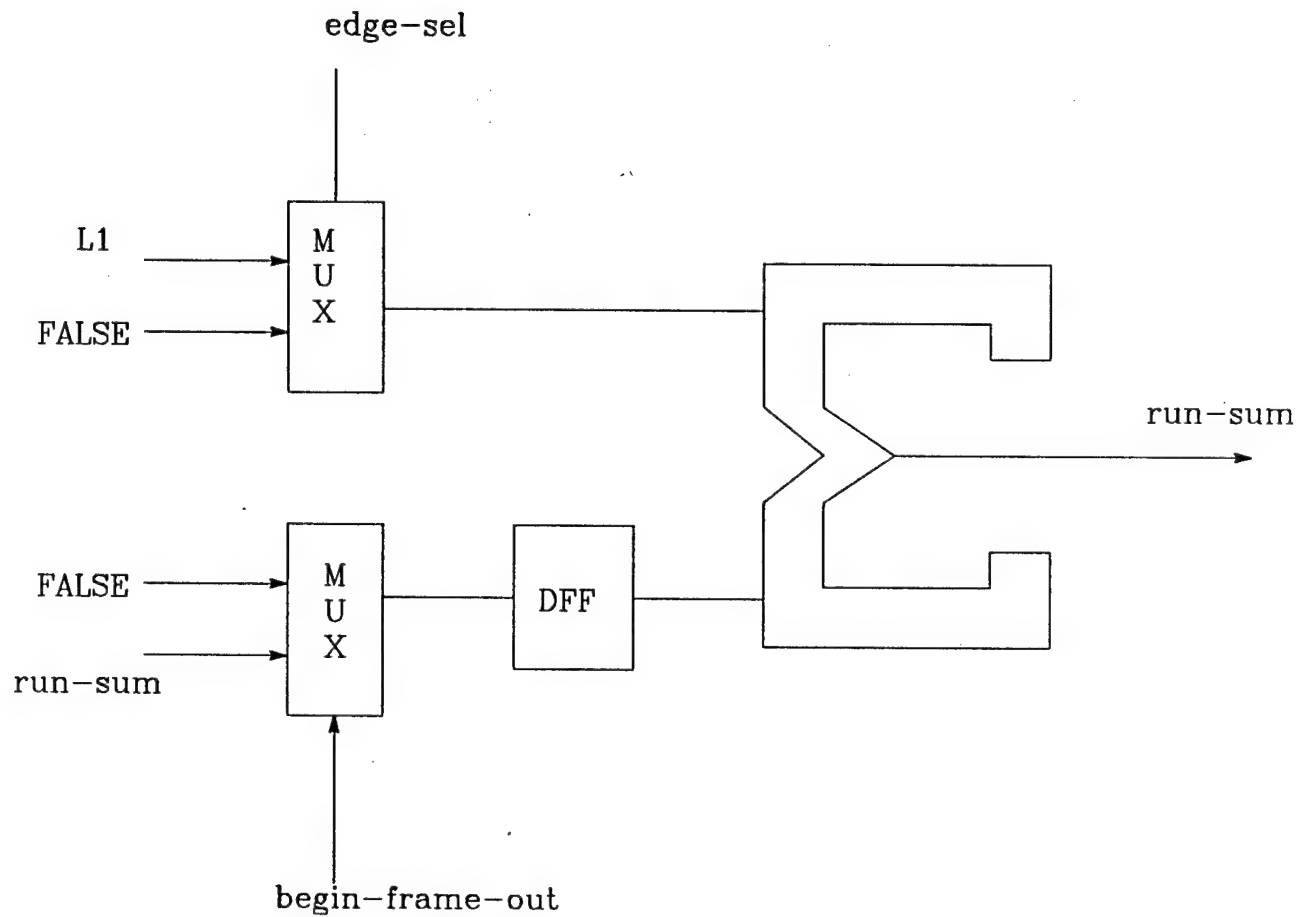


Figure 29. Running Sum Diagram

Appendix B. Pin Description

```

/*****
/*          Pin Description of GT-VTHR Thresholding Chip          */
*****/

```

PIN#	W/B#	ABBREVIATED NAME	SIGNAL_NAME	PAD_TYPE	TIMING
B2	1	VCC	VCC	VCC CORNER	
B1	2	Data[2]	Data[2]	DATA IO	SA/WA
C2	3	Data[3]	Data[3]	DATA IO	SA/WA
C1	4	VSS	VSS	VSS RING	
D2	5	Data[4]	Data[4]	DATA IO	SA/WA
D1	6	Data[5]	Data[5]	DATA IO	SA/WA
E2	7	Data[6]	Data[6]	DATA IO	SA/WA
E1	8	Data[7]	Data[7]	DATA IO	SA/WA
F3	9	VCC	VCC	VCC RING	
F2	10	Data[8]	Data[8]	DATA IO	SA/WA
F1	11	Data[9]	Data[9]	DATA IO	SA/WA
G2	12	Data[10]	Data[10]	DATA IO	SA/WA
G3	13	Data[11]	Data[11]	DATA IO	SA/WA
G1	14	VCC	VCC	VCC RING	
H1	15	Data[12]	Data[12]	DATA IO	SA/WA
H2	16	Data[13]	Data[13]	DATA IO	SA/WA
H3	17	Data[14]	Data[14]	DATA IO	SA/WA
J1	18	Data[15]	Data[15]	DATA IO	SA/WA
J2	19	VSS	VSS	VSS RING	
K1	20	Theta16	Theta16	DATA OUT	SA
K2	21	Erow_O	End_row_out	DATA OUT	SA
L1	22	Efrm_O	End_frame_out	DATA OUT	SA
M1	23	VCC	VCC	VCC RING	
L2	24	Brow_O	Begin_row_out	DATA OUT	SA
N1	25	-			
M2	26	VSS	VSS	VSS CORNER	
N2	27	Bfrm_O	Begin_frame_out	DATA OUT	SA
M3	28	Pxl_I[0]	Pixel_in[0]	DATA IN	VB
N3	29	Pxl_I[1]	Pixel_in[1]	DATA IN	VB
M4	30	Pxl_I[2]	Pixel_in[2]	DATA IN	VB
N4	31	Pxl_I[3]	Pixel_in[3]	DATA IN	VB
M5	32	Pxl_I[4]	Pixel_in[4]	DATA IN	VB
N5	33	VCC	VCC	VCC CORE	
L6	34	Pxl_I[5]	Pixel_in[5]	DATA IN	VB
M6	35	Pxl_I[6]	Pixel_in[6]	DATA IN	VB
N6	36	Pxl_I[7]	Pixel_in[7]	DATA IN	VB
M7	37	VCC	VCC	VCC CORE	
L7	38	Pxl_I[8]	Pixel_in[8]	DATA IN	VB
N7	39	Pxl_I[9]	Pixel_in[9]	DATA IN	VB
N8	40	VSS	VSS	VSS RING	
M8	41	Pxl_I[10]	Pixel_in[10]	DATA IN	VB
L8	42	Pxl_I[11]	Pixel_in[11]	DATA IN	VB
N9	43	Pxl_I[12]	Pixel_in[12]	DATA IN	VB
M9	44	Pxl_I[13]	Pixel_in[13]	DATA IN	VB
N10	45	Pxl_I[14]	Pixel_in[14]	DATA IN	VB
M10	46	Pxl_I[15]	Pixel_in[15]	DATA IN	VB
N11	47	Brow_I	Begin_row_in	DATA IN	VB
N12	48	Erow_I	End_row_in	DATA IN	VB
M11	49	Bfrm_I	Begin_frame_in	DATA IN	VB
N13	50	-			
M12	51	-			
M13	52	Efrm_I	End_frame_in	DATA IN	VB
L12	53	VCC	VCC	VCC RING	

L13	54	Pxl_O[0]	Pixel_out[0]	DATA OUT	SA
K12	55	Pxl_O[1]	Pixel_out[1]	DATA OUT	SA
K13	56	Pxl_O[2]	Pixel_out[2]	DATA OUT	SA
J12	57	Pxl_O[3]	Pixel_out[3]	DATA OUT	SA
J13	58	Pxl_O[4]	Pixel_out[4]	DATA OUT	SA
H11	59	Pxl_O[5]	Pixel_out[5]	DATA OUT	SA
H12	60	VSS	VSS	VSS RING	
H13	61	Pxl_O[6]	Pixel_out[6]	DATA OUT	SA
G12	62	Pxl_O[7]	Pixel_out[7]	DATA OUT	SA
G11	63	Pxl_O[8]	Pixel_out[8]	DATA OUT	SA
G13	64	Pxl_O[9]	Pixel_out[9]	DATA OUT	SA
F13	65	VCC	VCC	VCC RING	
F12	66	Pxl_O[10]	Pixel_out[10]	DATA OUT	SA
F11	67	Pxl_O[11]	Pixel_out[11]	DATA OUT	SA
E13	68	Pxl_O[12]	Pixel_out[12]	DATA OUT	SA
E12	69	Pxl_O[13]	Pixel_out[13]	DATA OUT	SA
D13	70	Pxl_O[14]	Pixel_out[14]	DATA OUT	SA
D12	71	Pxl_O[15]	Pixel_out[15]	DATA OUT	SA
C13	72	nReset	N_reset	DATA IN	WA
B13	73	VSS	VSS	VSS RING	
C12	74	ID[0]	Id[0]	DATA IN	WA
A13	75	VCC	VCC	VCC CORNER	
B12	76	ID[1]	Id[1]	DATA IN	WA
A12	77	ID[2]	Id[2]	DATA IN	WA
B11	78	VSS	VSS	VSS CORE	
A11	79	ID[3]	Id[3]	DATA IN	WA
B10	80	DS[0]	Ds[0]	DATA IN	WA
A10	81	DS[1]	Ds[1]	DATA IN	WA
B9	82	VCC	VCC	VCC RING	
A9	83	DS[2]	Ds[2]	DATA IN	WA
C8	84	DS[3]	Ds[3]	DATA IN	WA
B8	85	VCC	VCC	VCC CLOCK	
A8	86	VSS	VSS	VSS CLOCK	
B7	87	Pxl_Clk	Pixel_clk	CLOCK	
C7	88	IOS	Ios	DATA IN	VB
A7	89	Test	Test	DATA IN	VA
A6	90	ODE	Ode	DATA IN	WA
B6	91	DR -- see note (3)	N_dr	DATA OUT	PROP
C6	92	VSS	VSS	VSS CORE	
A5	93	Hadr[0]	Address[0]	DATA IN	WA
B5	94	Hadr[1]	Address[1]	DATA IN	WA
A4	95	Hadr[2]	Address[2]	DATA IN	WA
B4	96	Hadr[3]	Address[3]	DATA IN	WA
A3	97	Data[0]	Data[0]	DATA IO	SA/WA
A2	98	Data[1]	Data[1]	DATA IO	SA/WA
B3	99	VCC	VCC	VCC RING	
A1	100	-			

Note:

- (1) "W/B#" is the wire bond number. "PIN#" is the alphanumeric pin location.
- (2) TIMING = SA/WA means the I/O data pad has SA output and WA (VA+VB) input timing attribute.
- (3) DR is a propagational output which depends on WA inputs (DS, ID, ODE). The slowest path at worst case condition is 28.6 ns (from ID[0] to DR output).

Appendix C. Key Parameters

```

/*****
/*      Key Parameters Listing of Thresholding Chip (GT-VTHR)      */
*****/

KEY_PARAMETERS
)
) Key Parameters for Chip /mntb/theta/theta/theta
) =====
)
) TIME = Wed Feb 13 14:29:12 1991
)
) ROUTE_VERSION = 8.00
) HEIGHT = 404.9 MILS
)   ( = 10284.4 u )
) WIDTH = 400.0 MILS
)   ( = 10160.0 u )
) ROUTED = 1 (0=NO,1=YES)
) TOTAL_WIRE_LENGTH = 1393033 MILS
)   ( = 35383038. u )
) CORE_AREA = 130090.5 SQUARE_MILS
)   ( = 83929188.5 u2 )
) PADRING_AREA = 31878.0 SQUARE_MILS
)   ( = 20566410. u2 )
) PAD_AREA = 27478.8 SQUARE_MILS
)   ( = 17728223. u2 )
) ROUTE_AREA = 75467.1 SQUARE_MILS
)   ( = 48688356. u2 )
) PERCENT_ROUTING_OF_CORE = 58 %
) PERCENT_ROUTING_OF_CHIP = 46 %
) PERCENT_CORE_OF_CHIP = 80 %
) PERCENT_PADRING_OF_CHIP = 19 %
) PERCENT_PAD_OF_PADRING = 86 %
)
) NETLIST_VERSION = 2.0
) NETLIST_EXISTS = 1 (0=NO,1=YES)
)
) PHASE_A_TIME = 198.6 NANoseconds
) PHASE_B_TIME = 185.9 NANoseconds
) SYMMETRIC_TIME = 397.1 NANoseconds
) NUMBER_OF_TRANSISTORS = 123807
) POWER DISSIPATION = 853.03 MILLIWATTS @5V_10MHZ
)
)
) ROUTE_ESTIMATE_LVL = 0
) FLAT_ROUTE = 0 (0=NO,1=YES)
) TECHNOLOGY_NAME = CMOS-1
) PACKAGE_SPECIFIED = 0 (0=NO,1=YES)
) FABLINE_NAME = HP2_CN10B
) COMPILER_TYPE = GCX
)
) FLOORPLAN_VERSION = 8.0
) BOND_PAD_CNT = 96
) HEIGHT_ESTIMATE = 418.49 MILS
)   ( = 10629.64 u )
) WIDTH_ESTIMATE = 430.65 MILS
)   ( = 10938.50 u )
) FUSED = 1 (0=NO,1=YES)
) FUSION_REQUIRED = 1 (0=NO,1=YES)
) PINOUT = 1 (0=NO,1=YES)

```

```
) PINOUT_REQUIRED = 1 (0=NO,1=YES)
) PLACED = 1 (0=NO,1=YES)
) PLACEMENT_REQUIRED = 1 (0=NO,1=YES)
)
)
) AREA = 161960.0 SQUARE_MILS
)   ( = 104490115. u2 )
) OBJECT_TYPE = Chip
) AREA_PER_TRANSISTOR = 1.308165 SQUARE_MILS
)   ( = 843.975717 u2 )
) PHYSICAL_IMPLEMENTATIONS_EXIST = 0 (0=NO,1=YES)
) CHECKPOINTS_EXIST = 1 (0=NO,1=YES)
) CAN_SET_FABLINE = 1 (0=NO,1=YES)
)
) Key Parameter Listing Complete
```

Appendix D. PADRING.033

OUTPUT RINGS REPORT Version 1

Noise contribution:(ma/nh) Speed0: 2.50 Speed1: 5.00 Speed2: 8.33 Speed3: 16.66
 Limits: Maximum noise level: 100. Unacceptable level: 150

Combined power pads do not supply clean power to the core.
 Their use is discouraged

Ring under analysis: VDD

PAD NAME	EDGE	SPEED	DRIVE	PAD TYPE SUPPLY	COMMENT

sw_pad	SOUTH		POWER		
pixel_out[15]	WEST	1	CMOS	2	OK
pixel_out[14]	WEST	1	CMOS	2	OK
pixel_out[13]	WEST	1	CMOS	2	OK
pixel_out[12]	WEST	1	CMOS	2	OK
pixel_out[11]	WEST	1	CMOS	2	OK
pixel_out[10]	WEST	1	CMOS	2	OK
ring_vdd1[4]	WEST		POWER		
pixel_out[9]	WEST	1	CMOS	3	OK
pixel_out[8]	WEST	1	CMOS	3	OK
pixel_out[7]	WEST	1	CMOS	4	OK
pixel_out[6]	WEST	1	CMOS	4	OK
pixel_out[5]	WEST	1	CMOS	4	OK
pixel_out[4]	WEST	1	CMOS	4	OK
pixel_out[3]	WEST	1	CMOS	4	OK
pixel_out[2]	WEST	1	CMOS	4	OK
pixel_out[1]	WEST	1	CMOS	4	OK
pixel_out[0]	WEST	1	CMOS	5	OK
ring_vdd1[3]	WEST		POWER		
begin_frame_out	NORTH	1	CMOS	5	OK
begin_row_out	EAST	1	CMOS	5	OK
ring_vdd1[2]	EAST		POWER		
end_frame_out	EAST	1	CMOS	8	OK
end_row_out	EAST	1	CMOS	8	OK
tl6_pad	EAST	1	CMOS	6	OK
data_pads[15]	EAST	1	CMOS	6	OK
data_pads[14]	EAST	1	CMOS	6	OK
data_pads[13]	EAST	1	CMOS	6	OK
data_pads[12]	EAST	1	CMOS	6	OK
ring_vdd1[1]	EAST		POWER		
data_pads[11]	EAST	1	CMOS	6	OK
data_pads[10]	EAST	1	CMOS	5	OK
data_pads[9]	EAST	1	CMOS	5	OK
data_pads[8]	EAST	1	CMOS	4	OK
ring_vdd1[0]	EAST		POWER		
data_pads[7]	EAST	1	CMOS	4	OK
data_pads[6]	EAST	1	CMOS	4	OK
data_pads[5]	EAST	1	CMOS	4	OK
data_pads[4]	EAST	1	CMOS	4	OK
data_pads[3]	EAST	1	CMOS	4	OK
data_pads[2]	EAST	1	CMOS	4	OK
se_pad	EAST		POWER		

ring_vddl[5]	SOUTH	POWER			
data_pads[1]	SOUTH	1 CMOS	3	OK	
data_pads[0]	SOUTH	1 CMOS	3	OK	
DR_pad	SOUTH	1 CMOS	3	OK	

This ring has 6 more VDD pads than it needs
 Ring under analysis: VSS

PAD NAME	EDGE	SPEED	DRIVE	PAD	COMMENT
			TYPE	SUPPLY	

ring_vss1[2]	WEST	POWER			
pixel_out[15]	WEST	1 CMOS	2	OK	
pixel_out[14]	WEST	1 CMOS	2	OK	
pixel_out[13]	WEST	1 CMOS	2	OK	
pixel_out[12]	WEST	1 CMOS	2	OK	
pixel_out[11]	WEST	1 CMOS	2	OK	
pixel_out[10]	WEST	1 CMOS	2	OK	
pixel_out[9]	WEST	1 CMOS	2	OK	
pixel_out[8]	WEST	1 CMOS	3	OK	
pixel_out[7]	WEST	1 CMOS	3	OK	
pixel_out[6]	WEST	1 CMOS	3	OK	
ring_vss1[1]	WEST	POWER			
pixel_out[5]	WEST	1 CMOS	3	OK	
pixel_out[4]	WEST	1 CMOS	3	OK	
pixel_out[3]	WEST	1 CMOS	3	OK	
pixel_out[2]	WEST	1 CMOS	3	OK	
pixel_out[1]	WEST	1 CMOS	3	OK	
pixel_out[0]	WEST	1 CMOS	3	OK	
begin_frame_out	NORTH	1 CMOS	3	OK	
ne_pad	NORTH	POWER			
begin_row_out	EAST	1 CMOS	3	OK	
end_frame_out	EAST	1 CMOS	4	OK	
end_row_out	EAST	1 CMOS	4	OK	
t16_pad	EAST	1 CMOS	2	OK	
data_pads[15]	EAST	1 CMOS	2	OK	
data_pads[14]	EAST	1 CMOS	2	OK	
data_pads[13]	EAST	1 CMOS	2	OK	
data_pads[12]	EAST	1 CMOS	2	OK	
data_pads[11]	EAST	1 CMOS	2	OK	
data_pads[10]	EAST	1 CMOS	2	OK	
data_pads[9]	EAST	1 CMOS	1	OK	
data_pads[8]	EAST	1 CMOS	1	OK	
data_pads[7]	EAST	1 CMOS	1	OK	
data_pads[6]	EAST	1 CMOS	1	OK	
data_pads[5]	EAST	1 CMOS	1	OK	
data_pads[4]	EAST	1 CMOS	1	OK	
ring_vss1[0]	EAST	POWER			
data_pads[3]	EAST	1 CMOS	1	OK	
data_pads[2]	EAST	1 CMOS	1	OK	
data_pads[1]	SOUTH	1 CMOS	1	OK	
data_pads[0]	SOUTH	1 CMOS	1	OK	
DR_pad	SOUTH	1 CMOS	1	OK	

This ring has 2 more VSS pads than it needs

Appendix E. Power Dissipation

```

/*****
/*      Power Dissipation of Thresholding Chip (GT-VTHR)      */
*****/

run TNET
DISP_POWER
POWER
) Clock Pixel_clk [clock=-9999]
) Reading Routing Data . . .
) INFO: longest net delay: 13.2ns
) Nets with delay longer than 10.0ns are recorded in ancillary file LONG_NET
) STD
) INFO: Nets loading, driving information can be found in ancillary file TA_NET
) STD
) Back-annotating route capacitance for block power calculation. . .
) Power for block test_pad: 0.00mW(DC) 0.24mW(AC)
) Power for block tl6_pad: 0.00mW(DC) 4.50mW(AC)
) Power for block sw_pad: 0.00mW(DC) 0.00mW(AC)
) Power for block store_ctrl: 0.00mW(DC) 9.21mW(AC)
) Power for block store/mem2/fifo2: 0.00mW(DC) 53.13mW(AC)
) W: Node store/mem2/fifo1/space_avail is not routed
) Power for block store/mem2/fifo1: 0.00mW(DC) 54.09mW(AC)
) Power for block store/mem1/fifo2: 0.00mW(DC) 55.25mW(AC)
) Power for block store/mem1/fifo1: 0.00mW(DC) 54.08mW(AC)
) Power for block store/latches: 0.00mW(DC) 30.24mW(AC)
) Power for block se_pad: 0.00mW(DC) 0.00mW(AC)
) Power for block ring_vss1: 0.00mW(DC) 0.00mW(AC)
) Power for block ring_vss0: 0.00mW(DC) 0.00mW(AC)
) Power for block ring_vdd1: 0.00mW(DC) 0.00mW(AC)
) Power for block ring_vdd0: 0.00mW(DC) 0.00mW(AC)
) Power for block reset_pad: 0.00mW(DC) 1.25mW(AC)
) Power for block pixel_out[9]: 0.00mW(DC) 4.50mW(AC)
) Power for block pixel_out[8]: 0.00mW(DC) 4.50mW(AC)
) Power for block pixel_out[7]: 0.00mW(DC) 4.50mW(AC)
) Power for block pixel_out[6]: 0.00mW(DC) 4.50mW(AC)
) Power for block pixel_out[5]: 0.00mW(DC) 4.50mW(AC)
) Power for block pixel_out[4]: 0.00mW(DC) 4.50mW(AC)
) Power for block pixel_out[3]: 0.00mW(DC) 4.50mW(AC)
) Power for block pixel_out[2]: 0.00mW(DC) 4.50mW(AC)
) Power for block pixel_out[1]: 0.00mW(DC) 4.50mW(AC)
) Power for block pixel_out[15]: 0.00mW(DC) 4.50mW(AC)
) Power for block pixel_out[14]: 0.00mW(DC) 4.50mW(AC)
) Power for block pixel_out[13]: 0.00mW(DC) 4.50mW(AC)
) Power for block pixel_out[12]: 0.00mW(DC) 4.50mW(AC)
) Power for block pixel_out[11]: 0.00mW(DC) 4.50mW(AC)
) Power for block pixel_out[10]: 0.00mW(DC) 4.50mW(AC)
) Power for block pixel_out[0]: 0.00mW(DC) 4.50mW(AC)
) Power for block pixel_in[9]: 0.00mW(DC) 0.34mW(AC)
) Power for block pixel_in[8]: 0.00mW(DC) 0.33mW(AC)
) Power for block pixel_in[7]: 0.00mW(DC) 0.36mW(AC)
) Power for block pixel_in[6]: 0.00mW(DC) 0.39mW(AC)
) Power for block pixel_in[5]: 0.00mW(DC) 0.39mW(AC)
) Power for block pixel_in[4]: 0.00mW(DC) 0.44mW(AC)
) Power for block pixel_in[3]: 0.00mW(DC) 0.46mW(AC)
) Power for block pixel_in[2]: 0.00mW(DC) 0.45mW(AC)
) Power for block pixel_in[1]: 0.00mW(DC) 0.54mW(AC)
) Power for block pixel_in[15]: 0.00mW(DC) 0.27mW(AC)
) Power for block pixel_in[14]: 0.00mW(DC) 0.28mW(AC)
) Power for block pixel_in[13]: 0.00mW(DC) 0.23mW(AC)

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) Power for block pixel_in[12]: 0.00mW(DC) 0.21mW(AC)
) Power for block pixel_in[11]: 0.00mW(DC) 0.23mW(AC)
) Power for block pixel_in[10]: 0.00mW(DC) 0.29mW(AC)
) Power for block pixel_in[0]: 0.00mW(DC) 0.54mW(AC)
) Power for block pixel_clk: 0.00mW(DC) 30.41mW(AC)
) Power for block output/state_mach: 0.00mW(DC) 0.58mW(AC)
) W: Node output/neuron/activity[7] is not routed
) W: Node output/neuron/activity[6] is not routed
) W: Node output/neuron/activity[5] is not routed
) W: Node output/neuron/activity[4] is not routed
) W: Node output/neuron/activity[3] is not routed
) W: Node output/neuron/activity[2] is not routed
) W: Node output/neuron/activity[1] is not routed
) W: Node output/neuron/activity[0] is not routed
) W: Node output/neuron/activity[16] is not routed
) W: Node output/neuron/activity[15] is not routed
) W: Node output/neuron/activity[14] is not routed
) W: Node output/neuron/activity[13] is not routed
) W: Node output/neuron/activity[12] is not routed
) W: Node output/neuron/activity[11] is not routed
) W: Node output/neuron/activity[10] is not routed
) W: Node output/neuron/activity[9] is not routed
) W: Node output/neuron/ADDA0_COUT is not routed
) W: Node output/neuron/activity[8] is not routed
) Power for block output/neuron: 0.00mW(DC) 2.10mW(AC)
) Power for block output/mux1: 0.00mW(DC) 10.07mW(AC)
) Power for block output/mux0: 0.00mW(DC) 4.48mW(AC)
) Power for block output/inverters: 0.00mW(DC) 0.84mW(AC)
) Power for block output/delay: 0.00mW(DC) 8.61mW(AC)
) Power for block ode_pad: 0.00mW(DC) 0.22mW(AC)
) Power for block nw_pad: 0.00mW(DC) 0.12mW(AC)
) Power for block ne_pad: 0.00mW(DC) 0.00mW(AC)
) Power for block ios_pad: 0.00mW(DC) 0.32mW(AC)
) Power for block host_stuff/reg2: 0.00mW(DC) 14.70mW(AC)
) Power for block host_stuff/reg1: 0.00mW(DC) 16.47mW(AC)
) Power for block host_stuff/reg0: 0.00mW(DC) 19.49mW(AC)
) W: Node host_stuff/pdp/PORT9_EXT1[17] is not routed
) W: Node host_stuff/pdp/PORT9_EXT1[15] is not routed
) W: Node host_stuff/pdp/PORT9_EXT1[14] is not routed
) W: Node host_stuff/pdp/PORT9_EXT1[9] is not routed
) W: Node host_stuff/pdp/PORT9_EXT1[13] is not routed
) W: Node host_stuff/pdp/PORT9_EXT1[8] is not routed
) W: Node host_stuff/pdp/PORT9_EXT1[12] is not routed
) W: Node host_stuff/pdp/PORT9_EXT1[7] is not routed
) W: Node host_stuff/pdp/PORT9_EXT1[11] is not routed
) W: Node host_stuff/pdp/PORT9_EXT1[6] is not routed
) W: Node host_stuff/pdp/PORT9_EXT1[10] is not routed
) W: Node host_stuff/pdp/PORT9_EXT1[5] is not routed
) W: Node host_stuff/pdp/PORT9_EXT1[4] is not routed
) W: Node host_stuff/pdp/PORT9_EXT1[3] is not routed
) W: Node host_stuff/pdp/PORT9_EXT1[2] is not routed
) W: Node host_stuff/pdp/PORT9_EXT1[1] is not routed
) W: Node host_stuff/pdp/PORT9_EXT1[0] is not routed
) W: Node host_stuff/pdp/ADDA0_COUT is not routed
) Power for block host_stuff/pdp: 0.00mW(DC) 2.05mW(AC)
) Power for block host_stuff/muxes: 0.00mW(DC) 10.26mW(AC)
) Power for block host_stuff/inverters: 0.00mW(DC) 0.50mW(AC)
) Power for block host_stuff/interface/wr_ctrl: 0.00mW(DC) 0.87mW(AC)
) Power for block host_stuff/interface/rd_ctrl: 0.00mW(DC) 1.17mW(AC)
) Power for block host_stuff/interface/dr_ctrl: 4.93mW(DC) 0.23mW(AC)
) Power for block host_stuff/decoder: 0.00mW(DC) 1.00mW(AC)
) Power for block host_stuff/d_out_mux: 0.00mW(DC) 5.36mW(AC)

) Power for block host_stuff/controls: 0.00mW(DC) 1.54mW(AC)
) Power for block end_row_out: 0.00mW(DC) 4.50mW(AC)
) Power for block end_row_in: 0.00mW(DC) 0.74mW(AC)
) Power for block end_frame_out: 0.00mW(DC) 4.50mW(AC)
) Power for block end_frame_in: 0.00mW(DC) 0.73mW(AC)
) Power for block data_pads[9]: 0.00mW(DC) 4.79mW(AC)
) Power for block data_pads[8]: 0.00mW(DC) 4.79mW(AC)
) Power for block data_pads[7]: 0.00mW(DC) 4.76mW(AC)
) Power for block data_pads[6]: 0.00mW(DC) 4.70mW(AC)
) Power for block data_pads[5]: 0.00mW(DC) 4.71mW(AC)
) Power for block data_pads[4]: 0.00mW(DC) 4.75mW(AC)
) Power for block data_pads[3]: 0.00mW(DC) 4.90mW(AC)
) Power for block data_pads[2]: 0.00mW(DC) 4.93mW(AC)
) Power for block data_pads[1]: 0.00mW(DC) 4.92mW(AC)
) Power for block data_pads[15]: 0.00mW(DC) 4.99mW(AC)
) Power for block data_pads[14]: 0.00mW(DC) 4.93mW(AC)
) Power for block data_pads[13]: 0.00mW(DC) 4.86mW(AC)
) Power for block data_pads[12]: 0.00mW(DC) 4.84mW(AC)
) Power for block data_pads[11]: 0.00mW(DC) 4.82mW(AC)
) Power for block data_pads[10]: 0.00mW(DC) 4.82mW(AC)
) Power for block data_pads[0]: 0.00mW(DC) 4.98mW(AC)
) Power for block core_vss: 0.00mW(DC) 0.00mW(AC)
) Power for block core_vdd: 0.00mW(DC) 0.00mW(AC)
) Power for block clocks_etc/state_mach: 0.00mW(DC) 0.71mW(AC)
) Power for block clocks_etc/sp_interface: 0.00mW(DC) 8.19mW(AC)
) Power for block clocks_etc/last_row: 0.00mW(DC) 0.79mW(AC)
) Power for block clocks_etc/first_row: 0.00mW(DC) 0.79mW(AC)
) Power for block clocks_etc/end_row_delay: 0.00mW(DC) 1.23mW(AC)
) Power for block clocks_etc/end_fr_delay: 0.00mW(DC) 0.66mW(AC)
) Power for block clocks_etc/beg_row_delay: 0.00mW(DC) 1.22mW(AC)
) Power for block clocks_etc/beg_fr_delay: 0.00mW(DC) 1.33mW(AC)
) Power for block begin_row_out: 0.00mW(DC) 4.50mW(AC)
) Power for block begin_row_in: 0.00mW(DC) 0.66mW(AC)
) Power for block begin_frame_out: 0.00mW(DC) 4.50mW(AC)
) Power for block begin_frame_in: 0.00mW(DC) 0.65mW(AC)
) Power for block adjust/logic3: 0.00mW(DC) 0.72mW(AC)
) Power for block adjust/logic2: 0.00mW(DC) 2.76mW(AC)
) Power for block adjust/logic11: 0.00mW(DC) 2.18mW(AC)
) Power for block adjust/logic10: 0.00mW(DC) 7.47mW(AC)
) Power for block adjust/logic0: 0.00mW(DC) 3.93mW(AC)
) Power for block adjust/invert3: 0.00mW(DC) 0.37mW(AC)
) Power for block adjust/invert2: 0.00mW(DC) 0.33mW(AC)
) Power for block adjust/invert1: 0.00mW(DC) 0.51mW(AC)
) Power for block adjust/invert0: 0.00mW(DC) 0.50mW(AC)
) W: Node adjust/add2/COUT is not routed
) Power for block adjust/add2: 0.00mW(DC) 2.53mW(AC)
) Power for block adjust/add1: 0.00mW(DC) 2.61mW(AC)
) W: Node adjust/add01/N2_N0[9] is not routed
) W: Node adjust/add01/N2_N0[8] is not routed
) W: Node adjust/add01/N2_N0[7] is not routed
) W: Node adjust/add01/N2_N0[6] is not routed
) W: Node adjust/add01/N2_N0[5] is not routed
) W: Node adjust/add01/N2_N0[4] is not routed
) W: Node adjust/add01/N2_N0[3] is not routed
) W: Node adjust/add01/N2_N0[15] is not routed
) W: Node adjust/add01/N2_N0[2] is not routed
) W: Node adjust/add01/N2_N0[1] is not routed
) W: Node adjust/add01/N2_N0[14] is not routed
) W: Node adjust/add01/N2_N0[0] is not routed
) W: Node adjust/add01/N2_N0[13] is not routed
) W: Node adjust/add01/N2_N0[12] is not routed
) W: Node adjust/add01/N2_N0[11] is not routed

) W: Node adjust/add01/N2_NO[10] is not routed
) Power for block adjust/add01: 0.00mW(DC) 2.16mW(AC)
) W: Node adjust/add00/N1_NO[9] is not routed
) W: Node adjust/add00/N1_NO[8] is not routed
) W: Node adjust/add00/N1_NO[7] is not routed
) W: Node adjust/add00/N1_NO[6] is not routed
) W: Node adjust/add00/N1_NO[5] is not routed
) W: Node adjust/add00/N1_NO[4] is not routed
) W: Node adjust/add00/N1_NO[3] is not routed
) W: Node adjust/add00/N1_NO[2] is not routed
) W: Node adjust/add00/N1_NO[1] is not routed
) W: Node adjust/add00/N1_NO[0] is not routed
) W: Node adjust/add00/N1_NO[15] is not routed
) W: Node adjust/add00/N1_NO[14] is not routed
) W: Node adjust/add00/N1_NO[13] is not routed
) W: Node adjust/add00/N1_NO[12] is not routed
) W: Node adjust/add00/N1_NO[11] is not routed
) W: Node adjust/add00/N1_NO[10] is not routed
) Power for block adjust/add00: 0.00mW(DC) 2.12mW(AC)
) Power for block addr_pads[3]: 0.00mW(DC) 0.38mW(AC)
) Power for block addr_pads[2]: 0.00mW(DC) 0.19mW(AC)
) Power for block addr_pads[1]: 0.00mW(DC) 0.76mW(AC)
) Power for block addr_pads[0]: 0.00mW(DC) 1.08mW(AC)
) W: Node adapt/v_add_1/ADDA1_COUT is not routed
) W: Node adapt/v_add_1/ADDA2_COUT is not routed
) W: Node adapt/v_add_1/ADDA0_COUT is not routed
) Power for block adapt/v_add_1: 0.00mW(DC) 7.44mW(AC)
) W: Node adapt/v_add_0/ADDA1_COUT is not routed
) W: Node adapt/v_add_0/ADDA2_COUT is not routed
) W: Node adapt/v_add_0/ADDA0_COUT is not routed
) Power for block adapt/v_add_0: 0.00mW(DC) 6.69mW(AC)
) W: Node adapt/run_sum/run_sum[2] is not routed
) W: Node adapt/run_sum/run_sum[1] is not routed
) W: Node adapt/run_sum/run_sum[0] is not routed
) W: Node adapt/run_sum/ADDA0_COUT is not routed
) Power for block adapt/run_sum: 0.00mW(DC) 6.61mW(AC)
) W: Node adapt/mult_k2/STICKY[1] is not routed
) W: Node adapt/mult_k2/STICKY[0] is not routed
) W: Node adapt/mult_k2/k2xL1[9] is not routed
) W: Node adapt/mult_k2/k2xL1[8] is not routed
) W: Node adapt/mult_k2/k2xL1[7] is not routed
) W: Node adapt/mult_k2/k2xL1[6] is not routed
) W: Node adapt/mult_k2/k2xL1[5] is not routed
) W: Node adapt/mult_k2/k2xL1[4] is not routed
) W: Node adapt/mult_k2/k2xL1[3] is not routed
) W: Node adapt/mult_k2/k2xL1[2] is not routed
) W: Node adapt/mult_k2/k2xL1[1] is not routed
) W: Node adapt/mult_k2/k2xL1[0] is not routed
) W: Node adapt/mult_k2/k2xL1[12] is not routed
) W: Node adapt/mult_k2/k2xL1[11] is not routed
) W: Node adapt/mult_k2/k2xL1[10] is not routed
) W: Node adapt/mult_k2/ZERO is not routed
) Power for block adapt/mult_k2: 0.00mW(DC) 38.48mW(AC)
) W: Node adapt/mult_k1/STICKY[1] is not routed
) W: Node adapt/mult_k1/STICKY[0] is not routed
) W: Node adapt/mult_k1/k1xavg[13] is not routed
) W: Node adapt/mult_k1/k1xavg[12] is not routed
) W: Node adapt/mult_k1/k1xavg[11] is not routed
) W: Node adapt/mult_k1/k1xavg[10] is not routed
) W: Node adapt/mult_k1/k1xavg[9] is not routed
) W: Node adapt/mult_k1/k1xavg[8] is not routed
) W: Node adapt/mult_k1/k1xavg[7] is not routed

```

) W: Node adapt/mult_k1/klxavg[6] is not routed
) W: Node adapt/mult_k1/klxavg[5] is not routed
) W: Node adapt/mult_k1/klxavg[4] is not routed
) W: Node adapt/mult_k1/klxavg[3] is not routed
) W: Node adapt/mult_k1/klxavg[2] is not routed
) W: Node adapt/mult_k1/klxavg[1] is not routed
) W: Node adapt/mult_k1/klxavg[0] is not routed
) W: Node adapt/mult_k1/ZERO is not routed
) Power for block adapt/mult_k1: 0.00mW(DC) 35.28mW(AC)
) W: Node adapt/k3_add/thresh[3] is not routed
) W: Node adapt/k3_add/thresh[2] is not routed
) W: Node adapt/k3_add/thresh[1] is not routed
) W: Node adapt/k3_add/thresh[0] is not routed
) W: Node adapt/k3_add/ADDA0_COUT is not routed
) Power for block adapt/k3_add: 0.00mW(DC) 7.57mW(AC)
) Power for block adapt/k2_ctrl1: 0.00mW(DC) 1.17mW(AC)
) Power for block adapt/k2_ctrl0: 0.00mW(DC) 1.63mW(AC)
) W: Node adapt/k2_alu/ADDA0_COUT is not routed
) Power for block adapt/k2_alu: 0.00mW(DC) 5.06mW(AC)
) W: Node adapt/k2_add/ADDA0_COUT is not routed
) Power for block adapt/k2_add: 0.00mW(DC) 3.24mW(AC)
) W: Node adapt/k1_add/ADDA0_COUT is not routed
) Power for block adapt/k1_add: 0.00mW(DC) 2.62mW(AC)
) Power for block adapt/avg_inv2: 0.00mW(DC) 4.19mW(AC)
) Power for block adapt/avg_inv1: 0.00mW(DC) 2.76mW(AC)
) Power for block adapt/avg_inv0: 0.00mW(DC) 3.33mW(AC)
) Power for block adapt/add_carries: 0.00mW(DC) 2.24mW(AC)
) Power for block adapt/abs_dif_7: 0.00mW(DC) 4.86mW(AC)
) Power for block adapt/abs_dif_6: 0.00mW(DC) 6.45mW(AC)
) Power for block adapt/abs_dif_5: 0.00mW(DC) 9.02mW(AC)
) Power for block adapt/abs_dif_4: 0.00mW(DC) 7.21mW(AC)
) Power for block adapt/abs_dif_3: 0.00mW(DC) 8.88mW(AC)
) Power for block adapt/abs_dif_2: 0.00mW(DC) 5.56mW(AC)
) Power for block adapt/abs_dif_1: 0.00mW(DC) 6.07mW(AC)
) Power for block adapt/abs_dif_0: 0.00mW(DC) 7.50mW(AC)
) Power for block adapt/MSTflag: 5.31mW(DC) 0.11mW(AC)
) W: Node adapt/L1_add/ADDSUB3_COUT is not routed
) W: Node adapt/L1_add/L1[21] is not routed
) W: Node adapt/L1_add/ADDA0_COUT is not routed
) Power for block adapt/L1_add: 0.00mW(DC) 10.12mW(AC)
) W: Node adapt/A0_3/ADDA1_COUT is not routed
) W: Node adapt/A0_3/ADDA3_COUT is not routed
) W: Node adapt/A0_3/ADDA2_COUT is not routed
) W: Node adapt/A0_3/ADDA0_COUT is not routed
) Power for block adapt/A0_3: 0.00mW(DC) 21.10mW(AC)
) Power for block ID_pads[3]: 0.00mW(DC) 0.28mW(AC)
) Power for block ID_pads[2]: 0.00mW(DC) 0.33mW(AC)
) Power for block ID_pads[1]: 0.00mW(DC) 0.35mW(AC)
) Power for block ID_pads[0]: 0.00mW(DC) 0.32mW(AC)
) Power for block DS_pads[3]: 0.00mW(DC) 0.23mW(AC)
) Power for block DS_pads[2]: 0.00mW(DC) 0.22mW(AC)
) Power for block DS_pads[1]: 0.00mW(DC) 0.28mW(AC)
) Power for block DS_pads[0]: 0.00mW(DC) 0.31mW(AC)
) Power for block DR_pad: 0.00mW(DC) 4.20mW(AC)
) Total power consumption (5.5V, 0 DegC 50pf/out_pad):
) DC: 10.24mW [10.24(core)+0.00(ring)]
) AC@10MHz: 836.69mW [629.97(core)+206.72(ring)]

```

TOTAL POWER : 846.93 mW

Appendix F. Timing and Simulation Setup Files

> worstcase.040:

```
LABEL Max junction T, min operating V
TEMP_VOLT 100 4.50
HOLDTIME_MARGIN 2.00
SELECT_EXT_CLOCK Pixel_clk
```

> nominal.040:

```
LABEL Room junction T, 5.0 operating V
TEMP_VOLT 55 5.00
HOLDTIME_MARGIN 2.00
SELECT_EXT_CLOCK Pixel_clk
```

> designinit.080:

```
func designinit {
    toggle Pixel_clk 0 '(0 5 10)
    tag Pixel_clk cycle rising
    tag Pixel_clk step both
    showtoggles
}
```

Appendix G. Timing Reports

Appendix G. 1. Pixel_Clk, GUARANTEED, Max T, Min V

```

*****
Genesil Version v8.0.2 -- Wed Feb 13 15:05:15 1991
Chip: /mntb/theta/theta/theta                                     Timing Analyzer
*****
CLOCK REPORT MODE
-----
Fabline: HP2_CN10B                      Corner: GUARANTEED
Junction Temperature:100 deg C          Voltage:4.50v
External Clock: Pixel_clk
Included setup files:
#0 worstcase                      (Max junction T, min operating V)
-----
-                                CLOCK TIMES (minimum)
Phase 1 High:  198.6  ns          Phase 2 High:  185.9  ns
-----
Cycle (from Ph1):  208.2  ns      Cycle (from Ph2):  249.5  ns
-----
Minimum Cycle Time:  384.5  ns      Symmetric Cycle Time:  397.1  ns
-----
-                                CLOCK WORST CASE PATHS
Minimum Phase 1 high time is  198.6  ns set by:
-----
** Clock delay: 7.4ns (206.0-198.6)
Node                               Cumulative Delay      Transition
pixel_out[2]/(internal)            206.0                  fall
pixel_out[2]/pixel_out              204.7                  rise
output/mux1/pixel_out[2]            204.2                  rise
output/mux1/pixel_out[2]'           190.2                  rise
output/mux1/NN_N6                   189.6                  fall
output/mux1/NNMUX213.SEL            189.0                  rise
output/mux1/NN_N1                   187.5                  fall
output/mux1/NN_N2                   186.4                  rise
output/mux1/n_state                 184.9                  fall
output/neuron/activity[17]          184.9                  fall
output/neuron/activity[17]'         184.7                  fall
output/neuron/ADDA0_OUT[17]         183.3                  fall
output/neuron/n_theta[16]           178.0                  fall
output/inverters/n_theta[16]        177.9                  fall
output/inverters/n_theta[16]'       176.9                  fall
output/inverters/theta[16]          176.3                  rise
output/mux0/theta[16]               176.3                  rise
output/mux0/theta[16]'              158.6                  rise
output/mux0/NN_N34                  158.1                  fall
output/mux0/adaptivel6              157.5                  rise
output/mux1/adaptivel6              157.5                  rise
output/mux1/adaptivel6'             152.5                  rise
output/mux1/n_adaptivel6            151.8                  fall
adapt/MSTflag/n_adaptivel6          149.6                  fall
adapt/MSTflag/n_adaptivel6'         141.8                  fall
adapt/MSTflag/thresh[20]            140.3                  rise
adapt/k3_add/thresh[24]             140.3                  rise
adapt/k3_add/thresh[24]'            140.1                  rise
adapt/k3_add/ADDA0_OUT[24]          138.8                  rise
adapt/k3_add/sum1[22]               131.3                  fall
adapt/k2_alu/sum1[22]               131.3                  fall

```

adapt/k2_alu/sum1[22]'	131.1	fall
adapt/k2_alu/ADDA0_OUT[22]	129.7	fall
adapt/k2_alu/sgn_prod2[18]	120.1	rise
adapt/k2_ctrl1/sgn_prod2[18]	120.0	rise
adapt/k2_ctrl1/sgn_prod2[18]'	114.7	rise
adapt/k2_ctrl1/n_prod2[18]	113.1	rise
adapt/k2_ctrl1/n_prod2[18]'	113.0	rise
adapt/k2_ctrl1/prod2[18]	112.1	fall
adapt/k2_add/k2xL1[32]	112.1	fall
adapt/k2_add/k2xL1[32]'	111.9	fall
adapt/k2_add/ADDA0_OUT[16]	110.4	fall
adapt/k2_add/k2xL10[0]	87.7	fall
adapt/mult_k2/k2xL10[0]	87.7	fall
adapt/mult_k2/k2xL10[0]'	86.2	fall
adapt/mult_k2/k2[0]	23.0	fall
host_stuff/reg0/k2[0]	22.5	fall
host_stuff/reg0/k2[0]'	17.7	fall
host_stuff/reg0/NNk21.clock_x	15.0	rise
host_stuff/reg0/PHASE_A	12.3	rise
pixel_clk/PHASE_A	11.2	rise
Pixel_clk	0.0	rise

Minimum Phase 2 high time is 185.9 ns set by:

 ** Clock delay: 7.0ns (192.9-185.9)

Node	Cumulative Delay	Transition
output/mux1/(internal)	192.9	rise
output/mux1/NNMUX213.SEL	190.6	fall
output/mux1/NN_N1	189.7	rise
output/mux1/NN_N2	188.4	fall
output/mux1/n_state	187.6	rise
output/neuron/activity[17]	187.6	rise
output/neuron/activity[17]'	187.4	rise
output/neuron/ADDA0_OUT[17]	186.1	rise
output/neuron/n_theta[16]	180.0	fall
output/inverters/n_theta[16]	180.0	fall
output/inverters/n_theta[16]'	178.9	fall
output/inverters/theta[16]	178.4	rise
output/mux0/theta[16]	178.4	rise
output/mux0/theta[16]'	160.6	rise
output/mux0/NN_N34	160.1	fall
output/mux0/adaptivel6	159.6	rise
output/mux1/adaptivel6	159.5	rise
output/mux1/adaptivel6'	154.5	rise
output/mux1/n_adaptivel6	153.9	fall
adapt/MSTflag/n_adaptivel6	151.6	fall
adapt/MSTflag/n_adaptivel6'	143.8	fall
adapt/MSTflag/thresh[20]	142.3	rise
adapt/k3_add/thresh[24]	142.3	rise
adapt/k3_add/thresh[24]'	142.1	rise
adapt/k3_add/ADDA0_OUT[24]	140.9	rise
adapt/k3_add/sum1[22]	133.3	fall
adapt/k2_alu/sum1[22]	133.3	fall
adapt/k2_alu/sum1[22]'	133.2	fall
adapt/k2_alu/ADDA0_OUT[22]	131.7	fall
adapt/k2_alu/sgn_prod2[18]	122.1	rise
adapt/k2_ctrl1/sgn_prod2[18]	122.1	rise
adapt/k2_ctrl1/sgn_prod2[18]'	116.7	rise
adapt/k2_ctrl1/n_prod2[18]	115.2	rise
adapt/k2_ctrl1/n_prod2[18]'	115.0	rise
adapt/k2_ctrl1/prod2[18]	114.1	fall
adapt/k2_add/k2xL1[32]	114.1	fall

adapt/k2_add/k2xL1[32]'	113.9	fall
adapt/k2_add/ADDA0_OUT[16]	112.4	fall
adapt/k2_add/k2xL10[0]	89.8	fall
adapt/mult_k2/k2xL10[0]	89.7	fall
adapt/mult_k2/k2xL10[0]'	88.2	fall
adapt/mult_k2/L1[3]	24.9	fall
adapt/L1_add/L1[3]	24.6	fall
adapt/L1_add/L1[3]'	19.8	fall
adapt/L1_add/INTER2_VAL1[3]	17.9	fall
adapt/L1_add/PHASE_B	13.3	rise
pixel_clk/PHASE_B	11.2	rise
Pixel_clk	0.0	fall

Minimum cycle time (from Ph1) is 208.2 ns set by:

 ** Clock delay: 12.1ns (220.3-208.2)

Node	Cumulative Delay	Transition
<put/mux1/NNCOUNTU4.mout_y[15]	220.3	rise
output/mux1/NN_N50	219.7	fall
output/mux1/NN_N3	219.1	rise
output/mux1/NN_N34	218.0	fall
<put/mux1/NNCOUNTU4.cout_y[13]	217.0	rise
output/mux1/NN_N33	216.0	fall
<put/mux1/NNCOUNTU4.cout_y[12]	215.2	rise
output/mux1/NN_N32	214.2	fall
<put/mux1/NNCOUNTU4.cout_y[11]	213.4	rise
output/mux1/NN_N31	212.4	fall
<put/mux1/NNCOUNTU4.cout_y[10]	211.7	rise
output/mux1/NN_N14	210.7	fall
<tput/mux1/NNCOUNTU4.cout_y[9]	210.1	rise
output/mux1/NN_N30	209.2	fall
<tput/mux1/NNCOUNTU4.cout_y[8]	208.5	rise
output/mux1/NN_N29	207.5	fall
<tput/mux1/NNCOUNTU4.cout_y[7]	206.8	rise
output/mux1/NN_N28	205.9	fall
<tput/mux1/NNCOUNTU4.cout_y[6]	205.2	rise
output/mux1/NN_N27	204.2	fall
<tput/mux1/NNCOUNTU4.cout_y[5]	203.6	rise
output/mux1/NN_N26	202.7	fall
<tput/mux1/NNCOUNTU4.cout_y[4]	202.0	rise
output/mux1/NN_N25	201.0	fall
<tput/mux1/NNCOUNTU4.cout_y[3]	200.2	rise
output/mux1/NN_N24	199.0	fall
<tput/mux1/NNCOUNTU4.cout_y[2]	198.3	rise
<tput/mux1/NNCOUNTU4.cout_y[1]	196.7	rise
output/mux1/NN_N22	195.8	fall
<tput/mux1/NNCOUNTU4.cout_y[0]	195.1	rise
output/mux1/NN_N21	194.1	fall
output/mux1/NNCOUNTU4.cin_y	193.5	rise
output/mux1/NNMUX213.SEL	191.5	rise
output/mux1/NN_N1	190.0	fall
output/mux1/NN_N2	189.0	rise
output/mux1/n_state	187.4	fall
output/neuron/activity[17]	187.4	fall
output/neuron/activity[17]'	187.3	fall
output/neuron/ADDA0_OUT[17]	185.8	fall
output/neuron/n_theta[16]	180.5	fall
output/inverters/n_theta[16]	180.5	fall
output/inverters/n_theta[16]'	179.4	fall
output/inverters/theta[16]	178.8	rise
output/mux0/theta[16]	178.8	rise
output/mux0/theta[16]'	161.1	rise

output/mux0/NN_N34	160.6	fall
output/mux0/adaptivel6	160.0	rise
output/mux1/adaptivel6	160.0	rise
output/mux1/adaptivel6'	155.0	rise
output/mux1/n_adaptivel6	154.4	fall
adapt/MSTflag/n_adaptivel6	152.1	fall
adapt/MSTflag/n_adaptivel6'	144.3	fall
adapt/MSTflag/thresh[20]	142.8	rise
adapt/k3_add/thresh[24]	142.8	rise
adapt/k3_add/thresh[24]'	142.6	rise
adapt/k3_add/ADDA0_OUT[24]	141.4	rise
adapt/k3_add/sum1[6]	117.1	fall
adapt/k2_alu/sum1[6]	117.1	fall
adapt/k2_alu/sum1[6]'	117.0	fall
adapt/k2_alu/ADDA0_OUT[6]	115.5	fall
adapt/k2_alu/INTER3_VAL1[4]	107.4	fall
*adapt/k2_alu/(internal)	104.7	fall
adapt/k2_alu/prod1[4]	102.7	fall
adapt/k1_add/k1xavg[18]	102.7	fall
adapt/k1_add/k1xavg[18]'	102.3	fall
adapt/k1_add/ADDA0_OUT[2]	100.8	fall
adapt/k1_add/k1xavg0[0]	92.7	fall
adapt/mult_k1/k1xavg0[0]	92.7	fall
adapt/mult_k1/k1xavg0[0]'	92.1	fall
adapt/mult_k1/k1[2]	25.7	fall
host_stuff/reg0/k1[2]	24.8	fall
host_stuff/reg0/k1[2]'	17.8	fall
host_stuff/reg0/NNk11.clock_x	15.0	rise
host_stuff/reg0/PHASE_A	12.3	rise
pixel_clk/PHASE_A	11.2	rise
Pixel_clk	0.0	rise

Minimum cycle time (from Ph2) is 249.5 ns set by:

** Clock delay: 7.0ns (256.5-249.5)

Node	Cumulative Delay	Transition
data_pads[15]/(internal)	256.5	fall
data_pads[15]/15	255.4	fall
data_pads[15]/data_out	255.1	rise
<stuff/d_out_mux/data_out[15]	254.6	rise
<stuff/d_out_mux/data_out[15]'	239.9	rise
host_stuff/d_out_mux/d_out[15]	238.3	rise
<st_stuff/d_out_mux/d_out[15]'	237.9	rise
host_stuff/d_out_mux/N0[15]	235.2	rise
output/mux1/N0[15]	234.5	rise
output/mux1/N0[15]'	221.7	rise
*<ut/mux1/NNCOUNTU4.mout_y[15]	219.8	rise
output/mux1/NN_N50	219.2	fall
output/mux1/NN_N3	218.6	rise
output/mux1/NN_N34	217.5	fall
<put/mux1/NNCOUNTU4.cout_y[13]	216.5	rise
output/mux1/NN_N33	215.5	fall
<put/mux1/NNCOUNTU4.cout_y[12]	214.8	rise
output/mux1/NN_N32	213.7	fall
<put/mux1/NNCOUNTU4.cout_y[11]	213.0	rise
output/mux1/NN_N31	212.0	fall
<put/mux1/NNCOUNTU4.cout_y[10]	211.2	rise
output/mux1/NN_N14	210.3	fall
<tput/mux1/NNCOUNTU4.cout_y[9]	209.6	rise
output/mux1/NN_N30	208.7	fall
<tput/mux1/NNCOUNTU4.cout_y[8]	208.0	rise
output/mux1/NN_N29	207.1	fall

<tput/mux1/NNCOUNTU4.cout_y[7]	206.4	rise
output/mux1/NN_N28	205.4	fall
<tput/mux1/NNCOUNTU4.cout_y[6]	204.8	rise
output/mux1/NN_N27	203.7	fall
<tput/mux1/NNCOUNTU4.cout_y[5]	203.1	rise
output/mux1/NN_N26	202.2	fall
<tput/mux1/NNCOUNTU4.cout_y[4]	201.5	rise
output/mux1/NN_N25	200.5	fall
<tput/mux1/NNCOUNTU4.cout_y[3]	199.8	rise
output/mux1/NN_N24	198.5	fall
<tput/mux1/NNCOUNTU4.cout_y[2]	197.8	rise
<tput/mux1/NNCOUNTU4.cout_y[1]	196.2	rise
output/mux1/NN_N22	195.3	fall
<tput/mux1/NNCOUNTU4.cout_y[0]	194.6	rise
output/mux1/NN_N21	193.6	fall
output/mux1/NNCOUNTU4.cin_y	193.0	rise
output/mux1/NNMUX213.SEL	191.1	rise
output/mux1/NN_N1	189.5	fall
output/mux1/NN_N2	188.5	rise
output/mux1/n_state	186.9	fall
output/neuron/activity[17]	186.9	fall
output/neuron/activity[17]'	186.8	fall
output/neuron/ADDA0_OUT[17]	185.3	fall
output/neuron/n_theta[16]	180.0	fall
output/inverters/n_theta[16]	180.0	fall
output/inverters/n_theta[16]'	178.9	fall
output/inverters/theta[16]	178.4	rise
output/mux0/theta[16]	178.4	rise
output/mux0/theta[16]'	160.6	rise
output/mux0/NN_N34	160.1	fall
output/mux0/adaptivel6	159.6	rise
output/mux1/adaptivel6	159.5	rise
output/mux1/adaptivel6'	154.5	rise
output/mux1/n_adaptivel6	153.9	fall
adapt/MSTflag/n_adaptivel6	151.6	fall
adapt/MSTflag/n_adaptivel6'	143.8	fall
adapt/MSTflag/thresh[20]	142.3	rise
adapt/k3_add/thresh[24]	142.3	rise
adapt/k3_add/thresh[24]'	142.1	rise
adapt/k3_add/ADDA0_OUT[24]	140.9	rise
adapt/k3_add/sum1[22]	133.3	fall
adapt/k2_alu/sum1[22]	133.3	fall
adapt/k2_alu/sum1[22]'	133.2	fall
adapt/k2_alu/ADDA0_OUT[22]	131.7	fall
adapt/k2_alu/sgn_prod2[18]	122.1	rise
adapt/k2_ctrl1/sgn_prod2[18]	122.1	rise
adapt/k2_ctrl1/sgn_prod2[18]'	116.7	rise
adapt/k2_ctrl1/n_prod2[18]	115.2	rise
adapt/k2_ctrl1/n_prod2[18]'	115.0	rise
adapt/k2_ctrl1/prod2[18]	114.1	fall
adapt/k2_add/k2xL1[32]	114.1	fall
adapt/k2_add/k2xL1[32]'	113.9	fall
adapt/k2_add/ADDA0_OUT[16]	112.4	fall
adapt/k2_add/k2xL10[0]	89.8	fall
adapt/mult_k2/k2xL10[0]	89.7	fall
adapt/mult_k2/k2xL10[0]'	88.2	fall
adapt/mult_k2/L1[3]	24.9	fall
adapt/L1_add/L1[3]	24.6	fall
adapt/L1_add/L1[3]'	19.8	fall
adapt/L1_add/INTER2_VAL1[3]	17.9	fall
adapt/L1_add/PHASE_B	13.3	rise
pixel_clk/PHASE_B	11.2	rise

Pixel_clk

0.0

fall

 Genesil Version v8.0.2 -- Wed Feb 13 16:51:58 1991
 Chip: /mntb/theta/theta/theta Timing Analyzer

 SETUP AND HOLD MODE

 Fabline: HP2_CN10B Corner: GUARANTEED
 Junction Temperature:100 deg C Voltage:4.50v
 External Clock: Pixel_clk
 Included setup files:
 #0 worstcase (Max junction T, min operating V)

Input	INPUT SETUP AND HOLD TIMES (ns)				PATH
	Setup Time		Hold Time		
	Ph1(f)	Ph2(f)	Ph1(f)	Ph2(f)	
Address[0]	39.3	21.2	-8.6	-12.3	PATH
Address[1]	37.3	19.1	-6.8	-11.6	PATH
Address[2]	29.6	15.3	-2.8	-7.3	PATH
Address[3]	34.7	20.5	-6.1	-12.8	PATH
Begin_frame_in	---	7.5	---	6.6	PATH
Begin_row_in	---	8.2	---	6.5	PATH
Data[0]	2.6	55.7	3.0	5.8	PATH
Data[10]	1.7	42.5	3.4	6.3	PATH
Data[11]	1.8	42.3	3.3	6.1	PATH
Data[12]	2.0	40.5	3.1	6.0	PATH
Data[13]	2.1	40.6	3.0	5.9	PATH
Data[14]	2.6	38.7	2.7	5.6	PATH
Data[15]	2.0	38.1	3.0	5.8	PATH
Data[1]	2.2	52.7	3.2	6.0	PATH
Data[2]	2.5	52.3	3.0	5.7	PATH
Data[3]	2.3	50.6	3.2	5.9	PATH
Data[4]	1.2	49.3	3.7	6.6	PATH
Data[5]	0.9	46.7	3.9	6.8	PATH
Data[6]	0.9	47.2	3.9	6.8	PATH
Data[7]	1.2	46.3	3.8	6.6	PATH
Data[8]	1.5	46.0	3.6	6.4	PATH
Data[9]	1.5	44.1	3.5	6.4	PATH
Ds[0]	34.7	27.1	-11.2	-7.2	PATH
Ds[1]	34.5	26.8	-11.0	-7.0	PATH
Ds[2]	34.1	26.5	-10.6	-6.6	PATH
Ds[3]	34.1	26.5	-10.7	-6.7	PATH
End_frame_in	---	7.4	---	6.5	PATH
End_row_in	---	9.6	---	6.6	PATH
Id[0]	34.9	27.2	-11.4	-7.4	PATH
Id[1]	34.1	26.4	-10.6	-6.6	PATH
Id[2]	34.1	26.4	-10.6	-6.6	PATH
Id[3]	34.9	27.2	-11.4	-7.4	PATH
Ios	---	3.9	---	-1.3	PATH
N_reset	19.6	18.3	-10.5	-8.6	PATH
Ode	31.5	22.8	-8.8	-4.4	PATH
Pixel_in[0]	---	2.7	---	6.2	PATH
Pixel_in[10]	---	1.8	---	6.4	PATH
Pixel_in[11]	---	1.4	---	6.4	PATH
Pixel_in[12]	---	1.4	---	6.4	PATH
Pixel_in[13]	---	1.6	---	6.5	PATH
Pixel_in[14]	---	1.9	---	6.5	PATH
Pixel_in[15]	---	1.8	---	6.5	PATH
Pixel_in[1]	---	2.8	---	6.2	PATH
Pixel_in[2]	---	1.9	---	6.2	PATH
Pixel_in[3]	---	3.6	---	6.3	PATH
Pixel_in[4]	---	2.0	---	6.3	PATH
Pixel_in[5]	---	3.0	---	6.3	PATH

Pixel_in[6]	---	3.0	---	6.3	PATH
Pixel_in[7]	---	2.6	---	6.4	PATH
Pixel_in[8]	---	2.4	---	6.4	PATH
Pixel_in[9]	---	2.5	---	6.4	PATH
Test	17.6	---	-1.0	---	PATH

 Genesil Version v8.0.2 -- Wed Feb 13 16:52:01 1991
 Chip: /mntb/theta/theta/theta Timing Analyzer

 OUTPUT DELAY MODE

 Fabline: HP2_CN10B Corner: GUARANTEED
 Junction Temperature:100 deg C Voltage:4.50v
 External Clock: Pixel_clk
 Included setup files:
 #0 worstcase (Max junction T, min operating V)

Output	OUTPUT DELAYS (ns)				Loading(pf)	
	Ph1(r) Delay		Ph2(r) Delay			
	Min	Max	Min	Max		
Begin_frame_out	---	---	22.1	25.9	50.00	PATH
Begin_row_out	---	---	22.0	25.8	50.00	PATH
Data[0]	---	---	21.0	24.8	50.00	PATH
Data[10]	---	---	21.6	25.4	50.00	PATH
Data[11]	---	---	21.7	25.4	50.00	PATH
Data[12]	---	---	21.8	25.5	50.00	PATH
Data[13]	---	---	21.8	25.6	50.00	PATH
Data[14]	---	---	21.8	25.6	50.00	PATH
Data[15]	---	---	21.9	25.6	50.00	PATH
Data[1]	---	---	21.0	24.8	50.00	PATH
Data[2]	---	---	21.2	25.0	50.00	PATH
Data[3]	---	---	21.2	25.0	50.00	PATH
Data[4]	---	---	21.3	25.1	50.00	PATH
Data[5]	---	---	21.3	25.1	50.00	PATH
Data[6]	---	---	21.4	25.2	50.00	PATH
Data[7]	---	---	21.5	25.2	50.00	PATH
Data[8]	---	---	21.6	25.3	50.00	PATH
Data[9]	---	---	21.6	25.4	50.00	PATH
End_frame_out	---	---	21.9	25.7	50.00	PATH
End_row_out	---	---	21.9	25.7	50.00	PATH
N_dr	18.6	34.1	18.6	28.6	50.00	PATH
Pixel_out[0]	---	---	22.3	26.1	50.00	PATH
Pixel_out[10]	---	---	21.7	25.5	50.00	PATH
Pixel_out[11]	---	---	21.6	25.4	50.00	PATH
Pixel_out[12]	---	---	21.5	25.3	50.00	PATH
Pixel_out[13]	---	---	21.4	25.2	50.00	PATH
Pixel_out[14]	---	---	21.3	25.1	50.00	PATH
Pixel_out[15]	---	---	21.2	25.0	50.00	PATH
Pixel_out[1]	---	---	22.2	26.0	50.00	PATH
Pixel_out[2]	---	---	22.2	26.0	50.00	PATH
Pixel_out[3]	---	---	22.1	25.9	50.00	PATH
Pixel_out[4]	---	---	22.1	25.9	50.00	PATH
Pixel_out[5]	---	---	22.0	25.9	50.00	PATH
Pixel_out[6]	---	---	21.9	25.8	50.00	PATH
Pixel_out[7]	---	---	21.9	25.7	50.00	PATH
Pixel_out[8]	---	---	21.8	25.7	50.00	PATH
Pixel_out[9]	---	---	21.8	25.6	50.00	PATH
Theta16	---	---	21.8	25.7	50.00	PATH

```
*****
Genesil Version v8.0.2 -- Wed Feb 13 16:53:17 1991
Chip: /mntb/theta/theta/theta                      Timing Analyzer
*****
VIOLATION MODE
-----
Fabline: HP2_CN10B                                Corner: GUARANTEED
Junction Temperature:100 deg C                     Voltage:4.50v
External Clock: Pixel_clk
Included setup files:
#0 worstcase                                     (Max junction T, min operating V)
-----
-                                         NO VIOLATIONS
Hold time check margin: 2.0ns
```

Appendix G. 2. Pixel_Clk, TYPICAL, Room T, 5.0 V

```

*****
Genesil Version v8.0.2 -- Wed Feb 13 17:07:28 1991
Chip: /mntb/theta/theta/theta                                     Timing Analyzer
*****
CLOCK REPORT MODE
-----
Fabline: HP2_CN10B                      Corner: TYPICAL
Junction Temperature:55 deg C           Voltage:5.00v
External Clock: Pixel_clk
Included setup files:
#0 nominal                             (Room junction T, 5.0 operating V)
-----
-                                CLOCK TIMES (minimum)
Phase 1 High:  102.5  ns           Phase 2 High:  95.6  ns
-----
Cycle (from Ph1):  108.1  ns       Cycle (from Ph2):  127.6  ns
-----
Minimum Cycle Time:  198.2  ns     Symmetric Cycle Time:  205.1  ns
-----
-                                CLOCK WORST CASE PATHS
Minimum Phase 1 high time is  102.5  ns set by:
-----
** Clock delay: 2.9ns (105.4-102.5)
Node                                Cumulative Delay      Transition
pixel_out[2]/(internal)             105.4                  fall
pixel_out[2]/pixel_out              104.7                  rise
output/mux1/pixel_out[2]            104.7                  rise
output/mux1/pixel_out[2]'           98.1                   rise
output/mux1/NN_N6                   97.7                   fall
output/mux1/NNMUX213.SEL            97.4                   rise
output/mux1/NN_N1                   96.6                   fall
output/mux1/NN_N2                   96.0                   rise
output/mux1/n_state                 95.2                   fall
output/neuron/activity[17]          95.2                   fall
output/neuron/activity[17]'         95.1                   fall
output/neuron/ADDA0_OUT[17]         94.3                   fall
output/neuron/n_theta[16]           91.5                   fall
output/inverters/n_theta[16]        91.5                   fall
output/inverters/n_theta[16]'       91.0                   fall
output/inverters/theta[16]          90.7                   rise
output/mux0/theta[16]               90.7                   rise
output/mux0/theta[16]'              82.2                   rise
output/mux0/NN_N34                  81.9                   fall
output/mux0/adaptivel6              81.6                   rise
output/mux1/adaptivel6              81.6                   rise
output/mux1/adaptivel6'              79.3                   rise
output/mux1/n_adaptivel6            78.9                   fall
adapt/MSTflag/n_adaptivel6          78.9                   fall
adapt/MSTflag/n_adaptivel6'         75.1                   fall
adapt/MSTflag/thresh[20]            74.2                   rise
adapt/k3_add/thresh[24]             74.2                   rise
adapt/k3_add/thresh[24]'            74.1                   rise
adapt/k3_add/ADDA0_OUT[24]          73.4                   rise
adapt/k3_add/sum1[22]               69.4                   fall
adapt/k2_alu/sum1[22]               69.4                   fall
adapt/k2_alu/sum1[22]'              69.3                   fall
adapt/k2_alu/ADDA0_OUT[22]          68.5                   fall
adapt/k2_alu/sgn_prod2[20]          64.6                   rise

```

adapt/k2_ctrl1/sgn_prod2[20]	64.6	rise
adapt/k2_ctrl1/sgn_prod2[20]'	62.0	rise
adapt/k2_ctrl1/n_prod2[20]	61.2	rise
adapt/k2_ctrl1/n_prod2[20]'	61.1	rise
adapt/k2_ctrl1/prod2[20]	60.6	fall
adapt/k2_add/k2xL1[34]	60.6	fall
adapt/k2_add/k2xL1[34]'	60.5	fall
adapt/k2_add/ADDA0_OUT[18]	59.7	fall
adapt/k2_add/k2xL10[0]	46.5	fall
adapt/mult_k2/k2xL10[0]	46.5	fall
adapt/mult_k2/k2xL10[0]'	45.7	fall
adapt/mult_k2/k2[0]	11.6	fall
host_stuff/reg0/k2[0]	11.6	fall
host_stuff/reg0/k2[0]'	9.1	fall
host_stuff/reg0/NNk21.clock_x	7.6	rise
host_stuff/reg0/PHASE_A	6.1	rise
pixel_clk/PHASE_A	6.1	rise
Pixel_clk	0.0	rise

Minimum Phase 2 high time is 95.6 ns set by:

 ** Clock delay: 3.2ns (98.8-95.6)

Node	Cumulative Delay	Transition
output/mux1/(internal)	98.8	rise
output/mux1/NNMUX213.SEL	97.6	fall
output/mux1/NN_N1	97.0	rise
output/mux1/NN_N2	96.3	fall
output/mux1/n_state	95.9	rise
output/neuron/activity[17]	95.9	rise
output/neuron/activity[17]'	95.8	rise
output/neuron/ADDA0_OUT[17]	95.1	rise
output/neuron/n_theta[16]	91.9	fall
output/inverters/n_theta[16]	91.9	fall
output/inverters/n_theta[16]'	91.3	fall
output/inverters/theta[16]	91.0	rise
output/mux0/theta[16]	91.0	rise
output/mux0/theta[16]'	82.5	rise
output/mux0/NN_N34	82.3	fall
output/mux0/adaptive16	82.0	rise
output/mux1/adaptive16	82.0	rise
output/mux1/adaptive16'	79.6	rise
output/mux1/n_adaptive16	79.3	fall
adapt/MSTflag/n_adaptive16	79.3	fall
adapt/MSTflag/n_adaptive16'	75.4	fall
adapt/MSTflag/thresh[20]	74.6	rise
adapt/k3_add/thresh[24]	74.6	rise
adapt/k3_add/thresh[24]'	74.5	rise
adapt/k3_add/ADDA0_OUT[24]	73.8	rise
adapt/k3_add/sum1[22]	69.7	fall
adapt/k2_alu/sum1[22]	69.7	fall
adapt/k2_alu/sum1[22]'	69.7	fall
adapt/k2_alu/ADDA0_OUT[22]	68.9	fall
adapt/k2_alu/sgn_prod2[20]	64.9	rise
adapt/k2_ctrl1/sgn_prod2[20]	64.9	rise
adapt/k2_ctrl1/sgn_prod2[20]'	62.3	rise
adapt/k2_ctrl1/n_prod2[20]	61.5	rise
adapt/k2_ctrl1/n_prod2[20]'	61.4	rise
adapt/k2_ctrl1/prod2[20]	60.9	fall
adapt/k2_add/k2xL1[34]	60.9	fall
adapt/k2_add/k2xL1[34]'	60.8	fall
adapt/k2_add/ADDA0_OUT[18]	60.0	fall
adapt/k2_add/k2xL10[0]	46.8	fall

adapt/mult_k2/k2xL10[0]	46.8	fall
adapt/mult_k2/k2xL10[0]'	46.0	fall
adapt/mult_k2/L1[3]	11.9	fall
adapt/L1_add/L1[3]	11.9	fall
adapt/L1_add/L1[3]'	9.3	fall
adapt/L1_add/INTER2_VAL1[3]	8.3	fall
adapt/L1_add/PHASE_B	5.8	rise
pixel_clk/PHASE_B	5.8	rise
Pixel_clk	0.0	fall

Minimum cycle time (from Ph1) is 108.1 ns set by:

 ** Clock delay: 6.1ns (114.3-108.1)

Node	Cumulative Delay	Transition
<put/mux1/NNCOUNTU4.mout_y[15]	114.3	rise
output/mux1/NN_N50	114.0	fall
output/mux1/NN_N3	113.6	rise
output/mux1/NN_N34	113.0	fall
<put/mux1/NNCOUNTU4.cout_y[13]	112.5	rise
output/mux1/NN_N33	112.0	fall
<put/mux1/NNCOUNTU4.cout_y[12]	111.6	rise
output/mux1/NN_N32	111.0	fall
<put/mux1/NNCOUNTU4.cout_y[11]	110.6	rise
output/mux1/NN_N31	110.1	fall
<put/mux1/NNCOUNTU4.cout_y[10]	109.7	rise
output/mux1/NN_N14	109.2	fall
<tput/mux1/NNCOUNTU4.cout_y[9]	108.8	rise
output/mux1/NN_N30	108.3	fall
<tput/mux1/NNCOUNTU4.cout_y[8]	108.0	rise
output/mux1/NN_N29	107.5	fall
<tput/mux1/NNCOUNTU4.cout_y[7]	107.1	rise
output/mux1/NN_N28	106.6	fall
<tput/mux1/NNCOUNTU4.cout_y[6]	106.2	rise
output/mux1/NN_N27	105.7	fall
<tput/mux1/NNCOUNTU4.cout_y[5]	105.3	rise
output/mux1/NN_N26	104.9	fall
<tput/mux1/NNCOUNTU4.cout_y[4]	104.5	rise
output/mux1/NN_N25	104.0	fall
<tput/mux1/NNCOUNTU4.cout_y[3]	103.5	rise
output/mux1/NN_N24	102.9	fall
<tput/mux1/NNCOUNTU4.cout_y[2]	102.5	rise
<tput/mux1/NNCOUNTU4.cout_y[1]	101.7	rise
output/mux1/NN_N22	101.2	fall
<tput/mux1/NNCOUNTU4.cout_y[0]	100.8	rise
output/mux1/NN_N21	100.3	fall
output/mux1/NNCOUNTU4.cin_y	99.9	rise
output/mux1/NNMUX213.SEL	98.9	rise
output/mux1/NN_N1	98.1	fall
output/mux1/NN_N2	97.5	rise
output/mux1/n_state	96.7	fall
output/neuron/activity[17]	96.7	fall
output/neuron/activity[17]'	96.6	fall
output/neuron/ADDA0_OUT[17]	95.8	fall
output/neuron/n_theta[16]	93.0	fall
output/inverters/n_theta[16]	93.0	fall
output/inverters/n_theta[16]'	92.5	fall
output/inverters/theta[16]	92.1	rise
output/mux0/theta[16]	92.1	rise
output/mux0/theta[16]'	83.7	rise
output/mux0/NN_N34	83.4	fall
output/mux0/adaptivel6	83.1	rise
output/mux1/adaptivel6	83.1	rise

output/mux1/adaptive16'	80.7	rise
output/mux1/n_adaptive16	80.4	fall
adapt/MSTflag/n_adaptive16	80.4	fall
adapt/MSTflag/n_adaptive16'	76.5	fall
adapt/MSTflag/thresh[20]	75.7	rise
adapt/k3_add/thresh[24]	75.7	rise
adapt/k3_add/thresh[24]'	75.6	rise
adapt/k3_add/ADDA0_OUT[24]	74.9	rise
adapt/k3_add/sum1[6]	62.0	fall
adapt/k2_alu/sum1[6]	62.0	fall
adapt/k2_alu/sum1[6]'	61.9	fall
adapt/k2_alu/ADDA0_OUT[6]	61.1	fall
adapt/k2_alu/INTER3_VAL1[4]	56.8	fall
*adapt/k2_alu/(internal)	55.3	fall
adapt/k2_alu/prod1[4]	54.2	fall
adapt/k1_add/k1xavg[18]	54.2	fall
adapt/k1_add/k1xavg[18]'	54.1	fall
adapt/k1_add/ADDA0_OUT[2]	53.3	fall
adapt/k1_add/k1xavg0[0]	49.0	fall
adapt/mult_k1/k1xavg0[0]	49.0	fall
adapt/mult_k1/k1xavg0[0]'	48.7	fall
adapt/mult_k1/k1[2]	12.8	fall
host_stuff/reg0/k1[2]	12.8	fall
host_stuff/reg0/k1[2]'	9.1	fall
host_stuff/reg0/NNk11.clock_x	7.6	rise
host_stuff/reg0/PHASE_A	6.1	rise
pixel_clk/PHASE_A	6.1	rise
Pixel_clk	0.0	rise

Minimum cycle time (from Ph2) is 127.6 ns set by:

** Clock delay: 2.9ns (130.5-127.6)

Node	Cumulative Delay	Transition
data_pads[15]/(internal)	130.5	fall
data_pads[15]/15	129.9	fall
data_pads[15]/data_out	129.8	rise
<_stuff/d_out_mux/data_out[15]	129.8	rise
<stuff/d_out_mux/data_out[15]'	122.8	rise
host_stuff/d_out_mux/d_out[15]	122.0	rise
<st_stuff/d_out_mux/d_out[15]'	121.7	rise
host_stuff/d_out_mux/N0[15]	120.3	rise
output/mux1/N0[15]	120.3	rise
output/mux1/N0[15]'	114.2	rise
*<ut/mux1/NNCOUNTU4.mout_y[15]	113.2	rise
output/mux1/NN_N50	112.8	fall
output/mux1/NN_N3	112.5	rise
output/mux1/NN_N34	111.9	fall
<put/mux1/NNCOUNTU4.cout_y[13]	111.4	rise
output/mux1/NN_N33	110.9	fall
<put/mux1/NNCOUNTU4.cout_y[12]	110.4	rise
output/mux1/NN_N32	109.9	fall
<put/mux1/NNCOUNTU4.cout_y[11]	109.5	rise
output/mux1/NN_N31	109.0	fall
<put/mux1/NNCOUNTU4.cout_y[10]	108.6	rise
output/mux1/NN_N14	108.1	fall
<tput/mux1/NNCOUNTU4.cout_y[9]	107.7	rise
output/mux1/NN_N30	107.2	fall
<tput/mux1/NNCOUNTU4.cout_y[8]	106.8	rise
output/mux1/NN_N29	106.3	fall
<tput/mux1/NNCOUNTU4.cout_y[7]	106.0	rise
output/mux1/NN_N28	105.4	fall
<tput/mux1/NNCOUNTU4.cout_y[6]	105.1	rise

output/mux1/NN_N27	104.6	fall
<tput/mux1/NNCOUNTU4.cout_y[5]	104.2	rise
output/mux1/NN_N26	103.7	fall
<tput/mux1/NNCOUNTU4.cout_y[4]	103.4	rise
output/mux1/NN_N25	102.8	fall
<tput/mux1/NNCOUNTU4.cout_y[3]	102.4	rise
output/mux1/NN_N24	101.8	fall
<tput/mux1/NNCOUNTU4.cout_y[2]	101.4	rise
<tput/mux1/NNCOUNTU4.cout_y[1]	100.5	rise
output/mux1/NN_N22	100.1	fall
<tput/mux1/NNCOUNTU4.cout_y[0]	99.7	rise
output/mux1/NN_N21	99.2	fall
output/mux1/NNCOUNTU4.cin_y	98.8	rise
output/mux1/NNMUX213.SEL	97.8	rise
output/mux1/NN_N1	96.9	fall
output/mux1/NN_N2	96.4	rise
output/mux1/n_state	95.5	fall
output/neuron/activity[17]	95.5	fall
output/neuron/activity[17]'	95.5	fall
output/neuron/ADDA0_OUT[17]	94.7	fall
output/neuron/n_theta[16]	91.9	fall
output/inverters/n_theta[16]	91.9	fall
output/inverters/n_theta[16]'	91.3	fall
output/inverters/theta[16]	91.0	rise
output/mux0/theta[16]	91.0	rise
output/mux0/theta[16]'	82.5	rise
output/mux0/NN_N34	82.3	fall
output/mux0/adaptivel6	82.0	rise
output/mux1/adaptivel6	82.0	rise
output/mux1/adaptivel6'	79.6	rise
output/mux1/n_adaptivel6	79.3	fall
adapt/MSTflag/n_adaptivel6	79.3	fall
adapt/MSTflag/n_adaptivel6'	75.4	fall
adapt/MSTflag/thresh[20]	74.6	rise
adapt/k3_add/thresh[24]	74.6	rise
adapt/k3_add/thresh[24]'	74.5	rise
adapt/k3_add/ADDA0_OUT[24]	73.8	rise
adapt/k3_add/sum1[22]	69.7	fall
adapt/k2_alu/sum1[22]	69.7	fall
adapt/k2_alu/sum1[22]'	69.7	fall
adapt/k2_alu/ADDA0_OUT[22]	68.9	fall
adapt/k2_alu/sgn_prod2[20]	64.9	rise
adapt/k2_ctrl1/sgn_prod2[20]	64.9	rise
adapt/k2_ctrl1/sgn_prod2[20]'	62.3	rise
adapt/k2_ctrl1/n_prod2[20]	61.5	rise
adapt/k2_ctrl1/n_prod2[20]'	61.4	rise
adapt/k2_ctrl1/prod2[20]	60.9	fall
adapt/k2_add/k2xL1[34]	60.9	fall
adapt/k2_add/k2xL1[34]'	60.8	fall
adapt/k2_add/ADDA0_OUT[18]	60.0	fall
adapt/k2_add/k2xL10[0]	46.8	fall
adapt/mult_k2/k2xL10[0]	46.8	fall
adapt/mult_k2/k2xL10[0]'	46.0	fall
adapt/mult_k2/L1[3]	11.9	fall
adapt/L1_add/L1[3]	11.9	fall
adapt/L1_add/L1[3]'	9.3	fall
adapt/L1_add/INTER2_VAL1[3]	8.3	fall
adapt/L1_add/PHASE_B	5.8	rise
pixel_clk/PHASE_B	5.8	rise
Pixel_clk	0.0	fall

```

*****
Genesil Version v8.0.2 -- Wed Feb 13 18:54:05 1991
Chip: /mntb/theta/theta/theta                                     Timing Analyzer
*****
SETUP AND HOLD MODE

```

```

-----
Fabline: HP2_CN10B                      Corner: TYPICAL
Junction Temperature:55 deg C           Voltage:5.00v
External Clock: Pixel_clk
Included setup files:
#0 nominal                      (Room junction T, 5.0 operating V)
-----

```

	INPUT SETUP AND HOLD TIMES (ns)				
Input	Setup Time		Hold Time		
	Ph1(f)	Ph2(f)	Ph1(f)	Ph2(f)	
Address[0]	20.0	11.1	-5.0	-7.0	PATH
Address[1]	19.1	10.2	-4.0	-6.4	PATH
Address[2]	15.0	8.2	-1.7	-4.3	PATH
Address[3]	17.5	10.9	-3.6	-7.2	PATH
Begin_frame_in	---	4.1	---	1.9	PATH
Begin_row_in	---	4.1	---	1.9	PATH
Data[0]	1.6	28.9	1.1	2.7	PATH
Data[10]	1.2	22.0	1.3	3.0	PATH
Data[11]	1.2	21.7	1.3	3.0	PATH
Data[12]	1.3	20.8	1.3	2.9	PATH
Data[13]	1.3	20.7	1.2	2.9	PATH
Data[14]	1.5	19.7	1.1	2.8	PATH
Data[15]	1.1	19.3	1.3	3.0	PATH
Data[1]	1.5	27.3	1.2	2.8	PATH
Data[2]	1.5	27.0	1.1	2.8	PATH
Data[3]	1.4	26.1	1.2	2.9	PATH
Data[4]	1.1	25.6	1.4	3.1	PATH
Data[5]	1.0	24.3	1.4	3.1	PATH
Data[6]	0.9	24.6	1.4	3.1	PATH
Data[7]	1.1	24.0	1.4	3.1	PATH
Data[8]	1.2	23.8	1.3	3.0	PATH
Data[9]	1.2	22.8	1.3	3.0	PATH
Ds[0]	17.6	14.3	-6.2	-4.2	PATH
Ds[1]	17.5	14.2	-6.1	-4.1	PATH
Ds[2]	17.4	14.0	-6.0	-3.9	PATH
Ds[3]	17.4	14.0	-6.0	-3.9	PATH
End_frame_in	---	3.4	---	1.9	PATH
End_row_in	---	4.5	---	1.9	PATH
Id[0]	17.7	14.3	-6.3	-4.2	PATH
Id[1]	17.3	13.9	-5.8	-3.8	PATH
Id[2]	17.3	13.9	-5.9	-3.8	PATH
Id[3]	17.7	14.3	-6.3	-4.2	PATH
Ios	---	2.4	---	-1.0	PATH
N_reset	9.7	9.1	-5.8	-4.8	PATH
Ode	16.1	12.1	-5.1	-2.7	PATH
Pixel_in[0]	---	1.7	---	1.9	PATH
Pixel_in[10]	---	1.6	---	1.9	PATH
Pixel_in[11]	---	1.5	---	1.9	PATH
Pixel_in[12]	---	1.5	---	1.9	PATH
Pixel_in[13]	---	1.6	---	1.9	PATH
Pixel_in[14]	---	1.7	---	1.9	PATH
Pixel_in[15]	---	1.7	---	1.9	PATH
Pixel_in[1]	---	1.8	---	1.9	PATH
Pixel_in[2]	---	1.5	---	1.9	PATH
Pixel_in[3]	---	2.3	---	1.9	PATH
Pixel_in[4]	---	1.6	---	1.9	PATH
Pixel_in[5]	---	2.1	---	1.9	PATH

Pixel_in[6]	---	2.1	---	1.9	PATH
Pixel_in[7]	---	2.0	---	1.9	PATH
Pixel_in[8]	---	1.9	---	1.9	PATH
Pixel_in[9]	---	1.9	---	1.9	PATH
Test	9.1	---	-1.2	---	PATH

```
*****
Genesil Version v8.0.2 -- Wed Feb 13 18:54:08 1991
Chip: /mntb/theta/theta/theta                      Timing Analyzer
*****
OUTPUT DELAY MODE
```

```
-----
Fabline: HP2_CN10B                                Corner: TYPICAL
Junction Temperature:55 deg C                      Voltage:5.00v
External Clock: Pixel_clk
Included setup files:
#0 nominal                                (Room junction T, 5.0 operating V)
-----
```

Output	OUTPUT DELAYS (ns)				Loading(pf)	
	Ph1(r) Delay		Ph2(r) Delay			
	Min	Max	Min	Max		
Begin_frame_out	---	---	11.6	14.1	50.00	PATH
Begin_row_out	---	---	11.6	14.1	50.00	PATH
Data[0]	---	---	11.7	14.1	50.00	PATH
Data[10]	---	---	11.7	14.1	50.00	PATH
Data[11]	---	---	11.7	14.1	50.00	PATH
Data[12]	---	---	11.7	14.1	50.00	PATH
Data[13]	---	---	11.7	14.1	50.00	PATH
Data[14]	---	---	11.7	14.1	50.00	PATH
Data[15]	---	---	11.7	14.1	50.00	PATH
Data[1]	---	---	11.7	14.1	50.00	PATH
Data[2]	---	---	11.7	14.1	50.00	PATH
Data[3]	---	---	11.7	14.1	50.00	PATH
Data[4]	---	---	11.7	14.1	50.00	PATH
Data[5]	---	---	11.7	14.1	50.00	PATH
Data[6]	---	---	11.7	14.1	50.00	PATH
Data[7]	---	---	11.7	14.1	50.00	PATH
Data[8]	---	---	11.7	14.1	50.00	PATH
Data[9]	---	---	11.7	14.1	50.00	PATH
End_frame_out	---	---	11.6	14.1	50.00	PATH
End_row_out	---	---	11.6	14.1	50.00	PATH
N_dr	11.4	19.5	11.4	16.4	50.00	PATH
Pixel_out[0]	---	---	11.6	14.1	50.00	PATH
Pixel_out[10]	---	---	11.6	14.1	50.00	PATH
Pixel_out[11]	---	---	11.6	14.1	50.00	PATH
Pixel_out[12]	---	---	11.6	14.1	50.00	PATH
Pixel_out[13]	---	---	11.6	14.1	50.00	PATH
Pixel_out[14]	---	---	11.6	14.1	50.00	PATH
Pixel_out[15]	---	---	11.6	14.1	50.00	PATH
Pixel_out[1]	---	---	11.6	14.1	50.00	PATH
Pixel_out[2]	---	---	11.6	14.1	50.00	PATH
Pixel_out[3]	---	---	11.6	14.1	50.00	PATH
Pixel_out[4]	---	---	11.6	14.1	50.00	PATH
Pixel_out[5]	---	---	11.6	14.1	50.00	PATH
Pixel_out[6]	---	---	11.6	14.1	50.00	PATH
Pixel_out[7]	---	---	11.6	14.1	50.00	PATH
Pixel_out[8]	---	---	11.6	14.1	50.00	PATH
Pixel_out[9]	---	---	11.6	14.1	50.00	PATH
Theta16	---	---	11.6	14.1	50.00	PATH

```
*****
                        Genesil Version v8.0.2 -- Wed Feb 13 18:55:28 1991
Chip: /mntb/theta/theta/theta                               Timing Analyzer
*****
VIOLATION MODE
-----
Fabline: HP2_CN10B                      Corner: TYPICAL
Junction Temperature:55 deg C           Voltage:5.00v
External Clock: Pixel_clk
Included setup files:
#0 nominal                             (Room junction T, 5.0 operating V)
-----
-                                     NO VIOLATIONS
Hold time check margin: 2.0ns
```

Appendix G. 3. Pixel_Clk, GUARANTEED, Room T, 5.0 V

```

*****
Genesil Version v8.0.2 -- Wed Feb 13 19:11:09 1991
Chip: /mntb/theta/theta/theta                                     Timing Analyzer
*****
CLOCK REPORT MODE
-----
Fabline: HP2_CN10B                      Corner: GUARANTEED
Junction Temperature:55 deg C           Voltage:5.00v
External Clock: Pixel_clk
Included setup files:
#0 nominal                             (Room junction T, 5.0 operating V)
-----
-                                CLOCK TIMES (minimum)
Phase 1 High:  161.2  ns           Phase 2 High:  150.9  ns
-----
Cycle (from Ph1):  169.3  ns       Cycle (from Ph2):  202.6  ns
-----
Minimum Cycle Time:  312.1  ns     Symmetric Cycle Time:  322.3  ns
-----
-                                CLOCK WORST CASE PATHS
Minimum Phase 1 high time is  161.2  ns set by:
-----
** Clock delay: 6.0ns (167.2-161.2)
Node                                Cumulative Delay      Transition
pixel_out[2]/(internal)             167.2                 fall
pixel_out[2]/pixel_out              166.0                 rise
output/mux1/pixel_out[2]            165.7                 rise
output/mux1/pixel_out[2]'           154.4                 rise
output/mux1/NN_N6                   153.9                 fall
output/mux1/NNMUX213.SEL            153.4                 rise
output/mux1/NN_N1                   152.2                 fall
output/mux1/NN_N2                   151.3                 rise
output/mux1/n_state                 150.1                 fall
output/neuron/activity[17]          150.1                 fall
output/neuron/activity[17]'         150.0                 fall
output/neuron/ADDA0_OUT[17]         148.8                 fall
output/neuron/n_theta[16]           144.4                 fall
output/inverters/n_theta[16]        144.4                 fall
output/inverters/n_theta[16]'       143.6                 fall
output/inverters/theta[16]          143.1                 rise
output/mux0/theta[16]               143.1                 rise
output/mux0/theta[16]'              128.8                 rise
output/mux0/NN_N34                  128.4                 fall
output/mux0/adaptivel6               127.9                 rise
output/mux1/adaptivel6               127.9                 rise
output/mux1/adaptivel6'              123.9                 rise
output/mux1/n_adaptivel6             123.4                 fall
adapt/MSTflag/n_adaptivel6           121.5                 fall
adapt/MSTflag/n_adaptivel6'          115.3                 fall
adapt/MSTflag/thresh[20]             114.1                 rise
adapt/k3_add/thresh[24]              114.1                 rise
adapt/k3_add/thresh[24]'             113.9                 rise
adapt/k3_add/ADDA0_OUT[24]           112.9                 rise
adapt/k3_add/sum1[22]                106.6                 fall
adapt/k2_alu/sum1[22]                106.6                 fall
adapt/k2_alu/sum1[22]'               106.5                 fall
adapt/k2_alu/ADDA0_OUT[22]           105.3                 fall
adapt/k2_alu/sgn_prod2[18]           97.5                  rise

```

adapt/k2_ctrl1/sgn_prod2[18]	97.4	rise
adapt/k2_ctrl1/sgn_prod2[18]'	93.1	rise
adapt/k2_ctrl1/n_prod2[18]	91.8	rise
adapt/k2_ctrl1/n_prod2[18]'	91.7	rise
adapt/k2_ctrl1/prod2[18]	91.0	fall
adapt/k2_add/k2xL1[32]	91.0	fall
adapt/k2_add/k2xL1[32]'	90.8	fall
adapt/k2_add/ADDA0_OUT[16]	89.6	fall
adapt/k2_add/k2xL10[0]	71.0	fall
adapt/mult_k2/k2xL10[0]	71.0	fall
adapt/mult_k2/k2xL10[0]'	69.8	fall
adapt/mult_k2/k2[0]	18.6	fall
host_stuff/reg0/k2[0]	18.3	fall
host_stuff/reg0/k2[0]'	14.4	fall
host_stuff/reg0/NNk21.clock_x	12.2	rise
host_stuff/reg0/PHASE_A	10.0	rise
pixel_clk/PHASE_A	9.0	rise
Pixel_clk	0.0	rise

Minimum Phase 2 high time is 150.9 ns set by:

** Clock delay: 5.6ns (156.6-150.9)

Node	Cumulative Delay	Transition
output/mux1/(internal)	156.6	rise
output/mux1/NNMUX213.SEL	154.7	fall
output/mux1/NN_N1	154.0	rise
output/mux1/NN_N2	152.9	fall
output/mux1/n_state	152.3	rise
output/neuron/activity[17]	152.2	rise
output/neuron/activity[17]'	152.1	rise
output/neuron/ADDA0_OUT[17]	151.1	rise
output/neuron/n_theta[16]	146.0	fall
output/inverters/n_theta[16]	146.0	fall
output/inverters/n_theta[16]'	145.2	fall
output/inverters/theta[16]	144.7	rise
output/mux0/theta[16]	144.7	rise
output/mux0/theta[16]'	130.4	rise
output/mux0/NN_N34	130.0	fall
output/mux0/adaptive16	129.6	rise
output/mux1/adaptive16	129.5	rise
output/mux1/adaptive16'	125.5	rise
output/mux1/n_adaptive16	125.0	fall
adapt/MSTflag/n_adaptive16	123.2	fall
adapt/MSTflag/n_adaptive16'	116.9	fall
adapt/MSTflag/thresh[20]	115.7	rise
adapt/k3_add/thresh[24]	115.7	rise
adapt/k3_add/thresh[24]'	115.5	rise
adapt/k3_add/ADDA0_OUT[24]	114.5	rise
adapt/k3_add/sum1[22]	108.3	fall
adapt/k2_alu/sum1[22]	108.3	fall
adapt/k2_alu/sum1[22]'	108.2	fall
adapt/k2_alu/ADDA0_OUT[22]	107.0	fall
adapt/k2_alu/sgn_prod2[18]	99.1	rise
adapt/k2_ctrl1/sgn_prod2[18]	99.1	rise
adapt/k2_ctrl1/sgn_prod2[18]'	94.7	rise
adapt/k2_ctrl1/n_prod2[18]	93.5	rise
adapt/k2_ctrl1/n_prod2[18]'	93.3	rise
adapt/k2_ctrl1/prod2[18]	92.6	fall
adapt/k2_add/k2xL1[32]	92.6	fall
adapt/k2_add/k2xL1[32]'	92.5	fall
adapt/k2_add/ADDA0_OUT[16]	91.3	fall
adapt/k2_add/k2xL10[0]	72.7	fall

adapt/mult_k2/k2xL10[0]	72.7	fall
adapt/mult_k2/k2xL10[0]'	71.4	fall
adapt/mult_k2/L1[3]	20.1	fall
adapt/L1_add/L1[3]	19.9	fall
adapt/L1_add/L1[3]'	16.1	fall
adapt/L1_add/INTER2_VAL1[3]	14.5	fall
adapt/L1_add/PHASE_B	10.7	rise
pixel_clk/PHASE_B	9.0	rise
Pixel_clk	0.0	fall

Minimum cycle time (from Ph1) is 169.3 ns set by:

 ** Clock delay: 9.8ns (179.1-169.3)

Node	Cumulative Delay	Transition
<put/mux1/NNCOUNTU4.mout_y[15]	179.1	rise
output/mux1/NN_N50	178.5	fall
output/mux1/NN_N3	178.0	rise
output/mux1/NN_N34	177.2	fall
<put/mux1/NNCOUNTU4.cout_y[13]	176.4	rise
output/mux1/NN_N33	175.5	fall
<put/mux1/NNCOUNTU4.cout_y[12]	174.9	rise
output/mux1/NN_N32	174.1	fall
<put/mux1/NNCOUNTU4.cout_y[11]	173.4	rise
output/mux1/NN_N31	172.6	fall
<put/mux1/NNCOUNTU4.cout_y[10]	172.0	rise
output/mux1/NN_N14	171.2	fall
<tput/mux1/NNCOUNTU4.cout_y[9]	170.7	rise
output/mux1/NN_N30	170.0	fall
<tput/mux1/NNCOUNTU4.cout_y[8]	169.4	rise
output/mux1/NN_N29	168.6	fall
<tput/mux1/NNCOUNTU4.cout_y[7]	168.0	rise
output/mux1/NN_N28	167.2	fall
<tput/mux1/NNCOUNTU4.cout_y[6]	166.7	rise
output/mux1/NN_N27	165.9	fall
<tput/mux1/NNCOUNTU4.cout_y[5]	165.3	rise
output/mux1/NN_N26	164.6	fall
<tput/mux1/NNCOUNTU4.cout_y[4]	164.0	rise
output/mux1/NN_N25	163.2	fall
<tput/mux1/NNCOUNTU4.cout_y[3]	162.6	rise
output/mux1/NN_N24	161.6	fall
<tput/mux1/NNCOUNTU4.cout_y[2]	161.0	rise
<tput/mux1/NNCOUNTU4.cout_y[1]	159.7	rise
output/mux1/NN_N22	159.0	fall
<tput/mux1/NNCOUNTU4.cout_y[0]	158.4	rise
output/mux1/NN_N21	157.6	fall
output/mux1/NNCOUNTU4.cin_y	157.1	rise
output/mux1/NNMUX213.SEL	155.5	rise
output/mux1/NN_N1	154.3	fall
output/mux1/NN_N2	153.4	rise
output/mux1/n_state	152.1	fall
output/neuron/activity[17]	152.1	fall
output/neuron/activity[17]'	152.0	fall
output/neuron/ADDA0_OUT[17]	150.8	fall
output/neuron/n_theta[16]	146.5	fall
output/inverters/n_theta[16]	146.5	fall
output/inverters/n_theta[16]'	145.6	fall
output/inverters/theta[16]	145.1	rise
output/mux0/theta[16]	145.1	rise
output/mux0/theta[16]'	130.9	rise
output/mux0/NN_N34	130.4	fall
output/mux0/adaptivel6	130.0	rise
output/mux1/adaptivel6	130.0	rise

output/mux1/adaptivel6'	126.0	rise
output/mux1/n_adaptivel6	125.4	fall
adapt/MSTflag/n_adaptivel6	123.6	fall
adapt/MSTflag/n_adaptivel6'	117.4	fall
adapt/MSTflag/thresh[20]	116.1	rise
adapt/k3_add/thresh[24]	116.1	rise
adapt/k3_add/thresh[24]'	115.9	rise
adapt/k3_add/ADDA0_OUT[24]	114.9	rise
adapt/k3_add/sum1[6]	95.0	fall
adapt/k2_alu/sum1[6]	95.0	fall
adapt/k2_alu/sum1[6]'	94.9	fall
adapt/k2_alu/ADDA0_OUT[6]	93.7	fall
adapt/k2_alu/INTER3_VAL1[4]	87.1	fall
*adapt/k2_alu/(internal)	84.9	fall
adapt/k2_alu/prod1[4]	83.2	fall
adapt/k1_add/k1xavg[18]	83.2	fall
adapt/k1_add/k1xavg[18]'	82.9	fall
adapt/k1_add/ADDA0_OUT[2]	81.7	fall
adapt/k1_add/k1xavg0[0]	75.1	fall
adapt/mult_k1/k1xavg0[0]	75.1	fall
adapt/mult_k1/k1xavg0[0]'	74.6	fall
adapt/mult_k1/k1[2]	24.0	rise
host_stuff/reg0/k1[2]	23.3	rise
host_stuff/reg0/k1[2]'	13.5	rise
host_stuff/reg0/NNk11.clock_x	12.1	rise
host_stuff/reg0/PHASE_A	10.0	rise
pixel_clk/PHASE_A	9.0	rise
Pixel_clk	0.0	rise

Minimum cycle time (from Ph2) is 202.6 ns set by:

** Clock delay: 5.6ns (208.3-202.6)

Node	Cumulative Delay	Transition
data_pads[15]/(internal)	208.3	fall
data_pads[15]/15	207.4	fall
data_pads[15]/data_out	207.2	rise
<_stuff/d_out_mux/data_out[15]	206.7	rise
<stuff/d_out_mux/data_out[15]'	194.9	rise
host_stuff/d_out_mux/d_out[15]	193.6	rise
<st_stuff/d_out_mux/d_out[15]'	193.2	rise
host_stuff/d_out_mux/N0[15]	191.1	rise
output/mux1/N0[15]	190.5	rise
output/mux1/N0[15]'	180.2	rise
*<ut/mux1/NNCOUNTU4.mout_y[15]	178.6	rise
output/mux1/NN_N50	178.1	fall
output/mux1/NN_N3	177.6	rise
output/mux1/NN_N34	176.7	fall
<put/mux1/NNCOUNTU4.cout_y[13]	175.9	rise
output/mux1/NN_N33	175.1	fall
<put/mux1/NNCOUNTU4.cout_y[12]	174.5	rise
output/mux1/NN_N32	173.6	fall
<put/mux1/NNCOUNTU4.cout_y[11]	173.0	rise
output/mux1/NN_N31	172.2	fall
<put/mux1/NNCOUNTU4.cout_y[10]	171.6	rise
output/mux1/NN_N14	170.8	fall
<tput/mux1/NNCOUNTU4.cout_y[9]	170.3	rise
output/mux1/NN_N30	169.5	fall
<tput/mux1/NNCOUNTU4.cout_y[8]	168.9	rise
output/mux1/NN_N29	168.2	fall
<tput/mux1/NNCOUNTU4.cout_y[7]	167.6	rise
output/mux1/NN_N28	166.8	fall
<tput/mux1/NNCOUNTU4.cout_y[6]	166.3	rise

output/mux1/NN_N27	165.5	fall
<tput/mux1/NNCOUNTU4.cout_y[5]	164.9	rise
output/mux1/NN_N26	164.2	fall
<tput/mux1/NNCOUNTU4.cout_y[4]	163.6	rise
output/mux1/NN_N25	162.8	fall
<tput/mux1/NNCOUNTU4.cout_y[3]	162.2	rise
output/mux1/NN_N24	161.2	fall
<tput/mux1/NNCOUNTU4.cout_y[2]	160.6	rise
<tput/mux1/NNCOUNTU4.cout_y[1]	159.3	rise
output/mux1/NN_N22	158.5	fall
<tput/mux1/NNCOUNTU4.cout_y[0]	158.0	rise
output/mux1/NN_N21	157.2	fall
output/mux1/NNCOUNTU4.cin_y	156.7	rise
output/mux1/NNMUX213.SEL	155.1	rise
output/mux1/NN_N1	153.8	fall
output/mux1/NN_N2	153.0	rise
output/mux1/n_state	151.7	fall
output/neuron/activity[17]	151.7	fall
output/neuron/activity[17]'	151.6	fall
output/neuron/ADDA0_OUT[17]	150.4	fall
output/neuron/n_theta[16]	146.0	fall
output/inverters/n_theta[16]	146.0	fall
output/inverters/n_theta[16]'	145.2	fall
output/inverters/theta[16]	144.7	rise
output/mux0/theta[16]	144.7	rise
output/mux0/theta[16]'	130.4	rise
output/mux0/NN_N34	130.0	fall
output/mux0/adaptivel6	129.6	rise
output/mux1/adaptivel6	129.5	rise
output/mux1/adaptivel6'	125.5	rise
output/mux1/n_adaptivel6	125.0	fall
adapt/MSTflag/n_adaptivel6	123.2	fall
adapt/MSTflag/n_adaptivel6'	116.9	fall
adapt/MSTflag/thresh[20]	115.7	rise
adapt/k3_add/thresh[24]	115.7	rise
adapt/k3_add/thresh[24]'	115.5	rise
adapt/k3_add/ADDA0_OUT[24]	114.5	rise
adapt/k3_add/sum1[22]	108.3	fall
adapt/k2_alu/sum1[22]	108.3	fall
adapt/k2_alu/sum1[22]'	108.2	fall
adapt/k2_alu/ADDA0_OUT[22]	107.0	fall
adapt/k2_alu/sgn_prod2[18]	99.1	rise
adapt/k2_ctrl1/sgn_prod2[18]	99.1	rise
adapt/k2_ctrl1/sgn_prod2[18]'	94.7	rise
adapt/k2_ctrl1/n_prod2[18]	93.5	rise
adapt/k2_ctrl1/n_prod2[18]'	93.3	rise
adapt/k2_ctrl1/prod2[18]	92.6	fall
adapt/k2_add/k2xL1[32]	92.6	fall
adapt/k2_add/k2xL1[32]'	92.5	fall
adapt/k2_add/ADDA0_OUT[16]	91.3	fall
adapt/k2_add/k2xL10[0]	72.7	fall
adapt/mult_k2/k2xL10[0]	72.7	fall
adapt/mult_k2/k2xL10[0]'	71.4	fall
adapt/mult_k2/L1[3]	20.1	fall
adapt/L1_add/L1[3]	19.9	fall
adapt/L1_add/L1[3]'	16.1	fall
adapt/L1_add/INTER2_VAL1[3]	14.5	fall
adapt/L1_add/PHASE_B	10.7	rise
pixel_clk/PHASE_B	9.0	rise
Pixel_clk	0.0	fall

 Genesil Version v8.0.2 -- Wed Feb 13 21:08:56 1991
 Chip: /mntb/theta/theta/theta Timing Analyzer

 SETUP AND HOLD MODE

 Fabline: HP2_CN10B Corner: GUARANTEED
 Junction Temperature:55 deg C Voltage:5.00v
 External Clock: Pixel_clk
 Included setup files:
 #0 nominal (Room junction T, 5.0 operating V)

Input	INPUT SETUP AND HOLD TIMES (ns)				PATH
	Setup Time		Hold Time		
	Ph1(f)	Ph2(f)	Ph1(f)	Ph2(f)	
Address[0]	31.9	17.1	-6.9	-9.9	PATH
Address[1]	30.2	15.4	-5.5	-9.4	PATH
Address[2]	23.9	12.3	-2.3	-6.0	PATH
Address[3]	28.2	16.6	-5.0	-10.5	PATH
Begin_frame_in	---	6.1	---	5.3	PATH
Begin_row_in	---	6.7	---	5.3	PATH
Data[0]	2.1	45.3	2.4	4.7	PATH
Data[10]	1.4	34.6	2.7	5.1	PATH
Data[11]	1.5	34.4	2.7	5.0	PATH
Data[12]	1.7	32.9	2.5	4.9	PATH
Data[13]	1.8	33.0	2.4	4.8	PATH
Data[14]	2.2	31.4	2.2	4.5	PATH
Data[15]	1.7	31.0	2.4	4.7	PATH
Data[1]	1.8	42.9	2.6	4.9	PATH
Data[2]	2.1	42.6	2.4	4.7	PATH
Data[3]	1.9	41.2	2.5	4.8	PATH
Data[4]	1.0	40.1	3.0	5.4	PATH
Data[5]	0.8	38.0	3.1	5.5	PATH
Data[6]	0.8	38.4	3.2	5.5	PATH
Data[7]	1.0	37.7	3.0	5.4	PATH
Data[8]	1.2	37.4	2.9	5.2	PATH
Data[9]	1.3	35.8	2.8	5.2	PATH
Ds[0]	28.1	22.0	-9.2	-5.9	PATH
Ds[1]	27.9	21.8	-9.0	-5.7	PATH
Ds[2]	27.7	21.5	-8.7	-5.4	PATH
Ds[3]	27.7	21.5	-8.7	-5.5	PATH
End_frame_in	---	6.1	---	5.3	PATH
End_row_in	---	7.8	---	5.3	PATH
Id[0]	28.3	22.1	-9.3	-6.1	PATH
Id[1]	27.6	21.5	-8.7	-5.4	PATH
Id[2]	27.6	21.5	-8.7	-5.4	PATH
Id[3]	28.3	22.1	-9.3	-6.1	PATH
Ios	---	3.2	---	-1.1	PATH
N_reset	15.8	14.8	-8.5	-7.0	PATH
Ode	25.4	18.5	-7.2	-3.7	PATH
Pixel_in[0]	---	2.2	---	5.0	PATH
Pixel_in[10]	---	1.5	---	5.2	PATH
Pixel_in[11]	---	1.2	---	5.2	PATH
Pixel_in[12]	---	1.2	---	5.2	PATH
Pixel_in[13]	---	1.3	---	5.2	PATH
Pixel_in[14]	---	1.6	---	5.2	PATH
Pixel_in[15]	---	1.5	---	5.3	PATH
Pixel_in[1]	---	2.3	---	5.0	PATH
Pixel_in[2]	---	1.6	---	5.0	PATH
Pixel_in[3]	---	2.9	---	5.1	PATH
Pixel_in[4]	---	1.7	---	5.1	PATH
Pixel_in[5]	---	2.5	---	5.1	PATH

Pixel_in[6]	---	2.5	---	5.1	PATH
Pixel_in[7]	---	2.2	---	5.1	PATH
Pixel_in[8]	---	2.0	---	5.2	PATH
Pixel_in[9]	---	2.1	---	5.2	PATH
Test	14.3	---	-0.8	---	PATH

```
*****
Genesil Version v8.0.2 -- Wed Feb 13 21:13:13 1991
Chip: /mntb/theta/theta/theta                                     Timing Analyzer
*****
Critical Paths (setup/hold):
```

```
-----
Fabline: HP2_CN10B                      Corner: GUARANTEED
Junction Temperature:55 deg C           Voltage:5.00v
External Clock: Pixel_clk
Included setup files:
#0 nominal                      (Room junction T, 5.0 operating V)
-----
```

```
Phase 1, Setup time:    1.5ns (5.6-4.1)
host_stuff/reg2/(internal)           5.6      rise
host_stuff/reg2/data_in[11]          3.7      fall
data_pads[11]/data_in                3.2      fall
data_pads[11]/data_in'                2.0      fall
Data[11]                             0.0      fall
```

```
Phase 1, Hold time:     2.7ns (5.8-3.1)
host_stuff/reg0/data_in[11]          3.1      fall
data_pads[11]/data_in                2.9      fall
data_pads[11]/data_in'                1.7      fall
Data[11]                             0.0      fall
```

```
Phase 2, Setup time:    34.4ns (39.2-4.8)
output/mux1/(internal)               39.2      rise
output/mux1/NNMUX213.SEL             37.4      fall
output/mux1/NN_N1                    36.6      rise
output/mux1/NN_N2                    35.6      fall
output/mux1/n_state                  34.9      rise
output/neuron/activity[17]            34.9      rise
output/neuron/activity[17]'           34.7      rise
output/neuron/ADDA0_OUT[17]           33.7      rise
output/neuron/n_theta[11]             24.0      fall
output/inverters/n_theta[11]          24.0      fall
output/inverters/n_theta[11]'         22.8      fall
output/inverters/theta[11]            22.3      rise
output/mux0/theta[11]                 22.3      rise
output/mux0/theta[11]'                17.4      rise
output/mux0/NN_N2                    16.4      fall
output/mux0/simple[11]                15.6      rise
host_stuff/reg1/simple[11]            15.4      rise
host_stuff/reg1/simple[11]'           6.5      rise
host_stuff/reg1/data_in[11]           5.0      rise
data_pads[11]/data_in                4.5      rise
data_pads[11]/data_in'                2.3      rise
Data[11]                             0.0      rise
```

```
Phase 2, Hold time:     5.0ns (8.4-3.4)
host_stuff/reg2/data_in[11]          3.4      fall
data_pads[11]/data_in                2.9      fall
data_pads[11]/data_in'                1.7      fall
Data[11]                             0.0      fall
```

 Genesil Version v8.0.2 -- Wed Feb 13 21:17:22 1991
 Chip: /mntb/theta/theta/theta Timing Analyzer

Critical Paths (setup/hold):

 Fabline: HP2_CN10B Corner: GUARANTEED
 Junction Temperature: 55 deg C Voltage: 5.00v
 External Clock: Pixel_clk
 Included setup files:
 #0 nominal (Room junction T, 5.0 operating V)

Phase 1, Setup time: 1.4ns (5.5-4.1)
 host_stuff/reg2/(internal) 5.5 rise
 host_stuff/reg2/data_in[10] 3.6 fall
 data_pads[10]/data_in 3.1 fall
 data_pads[10]/data_in' 2.0 fall
 Data[10] 0.0 fall

Phase 1, Hold time: 2.7ns (5.7-3.0)
 host_stuff/reg0/data_in[10] 3.0 fall
 data_pads[10]/data_in 2.8 fall
 data_pads[10]/data_in' 1.7 fall
 Data[10] 0.0 fall

Phase 2, Setup time: 34.6ns (38.7-4.1)
 output/mux1/(internal) 38.7 rise
 output/mux1/NNMUX213.SEL 36.9 fall
 output/mux1/NN_N1 36.1 rise
 output/mux1/NN_N2 35.1 fall
 output/mux1/n_state 34.4 rise
 output/neuron/activity[17] 34.4 rise
 output/neuron/activity[17]' 34.3 rise
 output/neuron/ADDA0_OUT[17] 33.2 rise
 output/neuron/n_theta[10] 23.1 fall
 output/inverters/n_theta[10] 23.1 fall
 output/inverters/n_theta[10]' 21.7 fall
 output/inverters/theta[10] 21.2 rise
 output/mux0/theta[10] 21.2 rise
 output/mux0/theta[10]' 16.4 rise
 output/mux0/NN_N0 15.4 fall
 output/mux0/simple[10] 14.6 rise
 host_stuff/reg1/simple[10] 14.5 rise
 host_stuff/reg1/simple[10]' 6.4 rise
 host_stuff/reg1/data_in[10] 4.9 rise
 data_pads[10]/data_in 4.4 rise
 data_pads[10]/data_in' 2.3 rise
 Data[10] 0.0 rise

Phase 2, Hold time: 5.1ns (8.4-3.3)
 host_stuff/reg2/data_in[10] 3.3 fall
 data_pads[10]/data_in 2.8 fall
 data_pads[10]/data_in' 1.7 fall
 Data[10] 0.0 fall

```

*****
Genesil Version v8.0.2 -- Wed Feb 13 21:17:25 1991
Chip: /mntb/theta/theta/theta Timing Analyzer
*****
OUTPUT DELAY MODE
-----
Fabline: HP2_CN10B Corner: GUARANTEED
Junction Temperature:55 deg C Voltage:5.00v
External Clock: Pixel_clk
Included setup files:
#0 nominal (Room junction T, 5.0 operating V)
-----

```

Output	OUTPUT DELAYS (ns)				Loading(pf)	
	Ph1(r) Delay		Ph2(r) Delay			
	Min	Max	Min	Max		
Begin_frame_out	---	---	17.9	21.0	50.00	PATH
Begin_row_out	---	---	17.8	20.9	50.00	PATH
Data[0]	---	---	17.0	20.1	50.00	PATH
Data[10]	---	---	17.5	20.6	50.00	PATH
Data[11]	---	---	17.5	20.6	50.00	PATH
Data[12]	---	---	17.6	20.7	50.00	PATH
Data[13]	---	---	17.6	20.7	50.00	PATH
Data[14]	---	---	17.7	20.8	50.00	PATH
Data[15]	---	---	17.7	20.8	50.00	PATH
Data[1]	---	---	17.0	20.1	50.00	PATH
Data[2]	---	---	17.1	20.2	50.00	PATH
Data[3]	---	---	17.2	20.3	50.00	PATH
Data[4]	---	---	17.2	20.3	50.00	PATH
Data[5]	---	---	17.3	20.4	50.00	PATH
Data[6]	---	---	17.3	20.4	50.00	PATH
Data[7]	---	---	17.4	20.5	50.00	PATH
Data[8]	---	---	17.5	20.6	50.00	PATH
Data[9]	---	---	17.5	20.6	50.00	PATH
End_frame_out	---	---	17.7	20.9	50.00	PATH
End_row_out	---	---	17.7	20.8	50.00	PATH
N_dr	15.0	27.7	15.0	23.3	50.00	PATH
Pixel_out[0]	---	---	18.0	21.1	50.00	PATH
Pixel_out[10]	---	---	17.5	20.7	50.00	PATH
Pixel_out[11]	---	---	17.5	20.6	50.00	PATH
Pixel_out[12]	---	---	17.4	20.5	50.00	PATH
Pixel_out[13]	---	---	17.3	20.5	50.00	PATH
Pixel_out[14]	---	---	17.2	20.4	50.00	PATH
Pixel_out[15]	---	---	17.1	20.3	50.00	PATH
Pixel_out[1]	---	---	18.0	21.1	50.00	PATH
Pixel_out[2]	---	---	17.9	21.1	50.00	PATH
Pixel_out[3]	---	---	17.9	21.0	50.00	PATH
Pixel_out[4]	---	---	17.9	21.0	50.00	PATH
Pixel_out[5]	---	---	17.8	21.0	50.00	PATH
Pixel_out[6]	---	---	17.8	20.9	50.00	PATH
Pixel_out[7]	---	---	17.7	20.8	50.00	PATH
Pixel_out[8]	---	---	17.7	20.8	50.00	PATH
Pixel_out[9]	---	---	17.6	20.8	50.00	PATH
Theta16	---	---	17.7	20.8	50.00	PATH

Genesil Version v8.0.2 -- Wed Feb 13 21:18:44 1991
Chip: /mntb/theta/theta/theta Timing Analyzer

VIOLATION MODE

Fabline: HP2_CN10B Corner: GUARANTEED
Junction Temperature: 55 deg C Voltage: 5.00v
External Clock: Pixel_clk
Included setup files:
#0 nominal (Room junction T, 5.0 operating V)

- NO VIOLATIONS

Hold time check margin: 2.0ns